DATASHEET

BoT-nLE522

Specification

CONFIDENTEAL INFORMATION

chipsen

Revision History

Rev. No	Issued Date	Page	Description	Summary
V0.1	2017-06-07		Initial Release	

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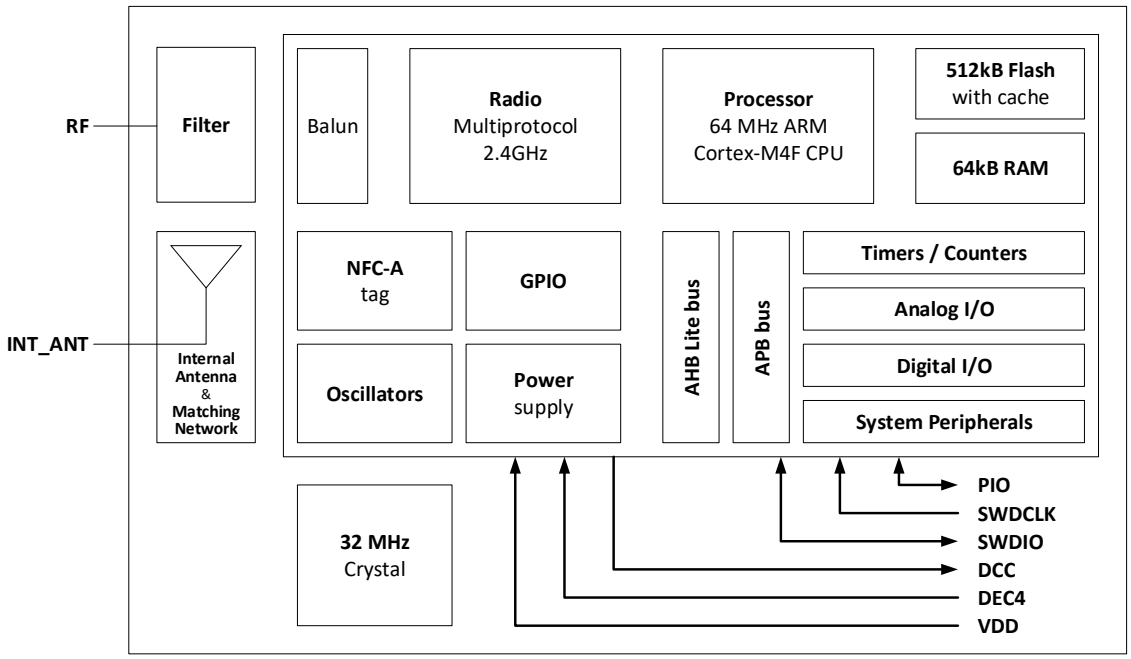
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1. General

1.1 Overview

The BoT-nLE522 module is a cost-effective, low-power, true system-on-chip (SoC) for Bluetooth Smart (Bluetooth low energy) applications. It enables robust BLE master or slave nodes to be built with very low total bill-of-material costs. BoT-nLE522 combines an excellent RF transceiver with an industry-standard enhanced Cortec-M4F CPU, in-system programmable flash memory, 64kB RAM, and many other powerful supporting features and peripherals. The BoT-nLE522 is suitable for systems where very low power
Consumption is required. Very low-power sleep modes are available. Short transition times between operating modes further enable low power consumption.



1.2 Features

■ Built in Antenna Bluetooth Smart (Bluetooth Low Energy) Module.

■ ARM® Cortex®-M4 32-bit processor with FPU, 64 MHz

■ Memory: 512 kB Flash/64 kB RAM

■ RF Output Power: MAX +4 dBm (-20 ~ 4 dBm)

■ RF Receive Sensitivity: -96 dBm

■ Type 2 near field communication (NFC-A) tag with wakeup-on-field and touch to-pair capabilities

■ Fully automatic LDO and DC/DC regulator system (Used LDO by Default)

■ Temperature Sensor

■ UART (CTS/RTS) with EasyDMA, SPI, and I2C data interfaces.

■ 12-Bit 200 ksps ADC with - 8 configurable channels with programmable gain

■ Size: 5 mm x 11 mm x 1.63 mm

■ Operating Voltage: 1.7V to 3.6V

■ Operating Temperature: -40 to +85℃

■ RoHS compliant

1.3 Application

■ 2.4 GHz Bluetooth Low Energy Systems

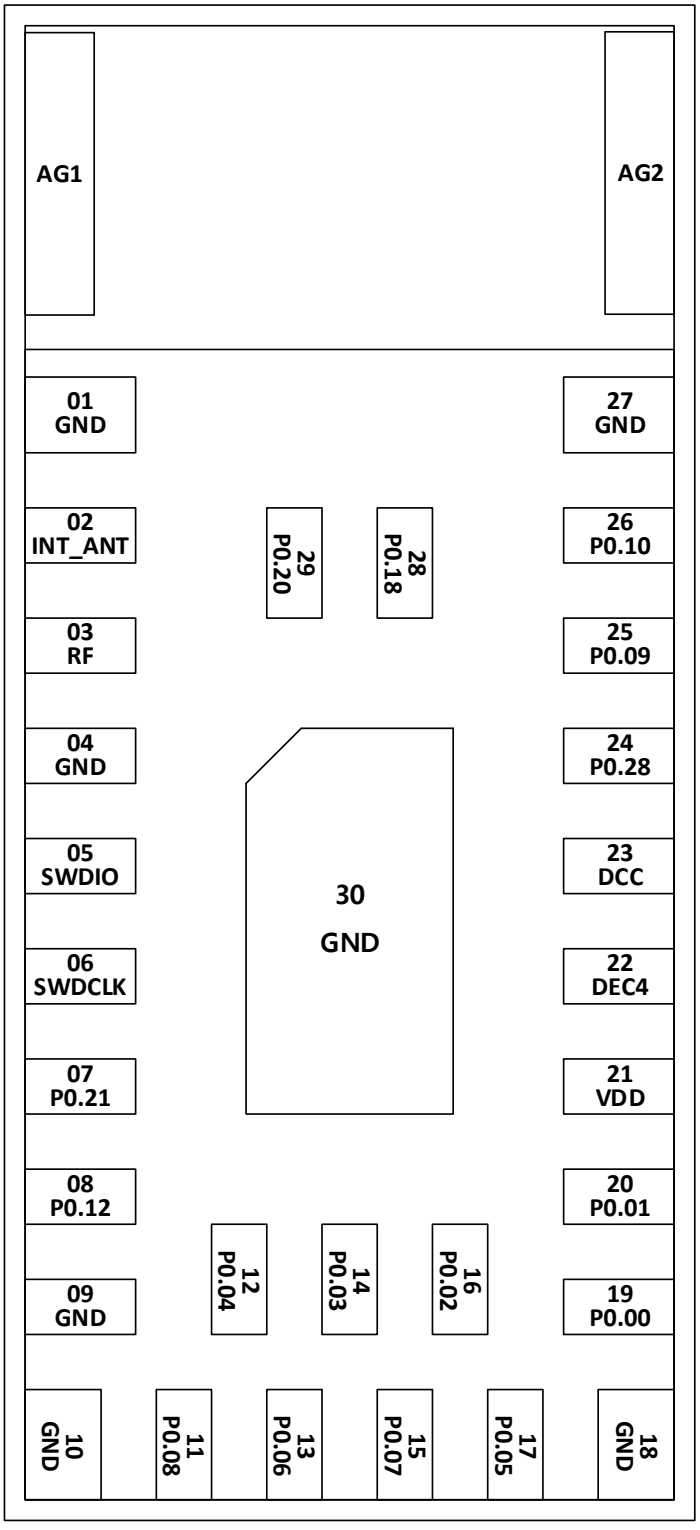
■ Human-Interface Devices

■ Sports and Leisure Equipment

■ Mobile Phone Accessories

■ Consumer Electronics

1.4 Pin Configuration

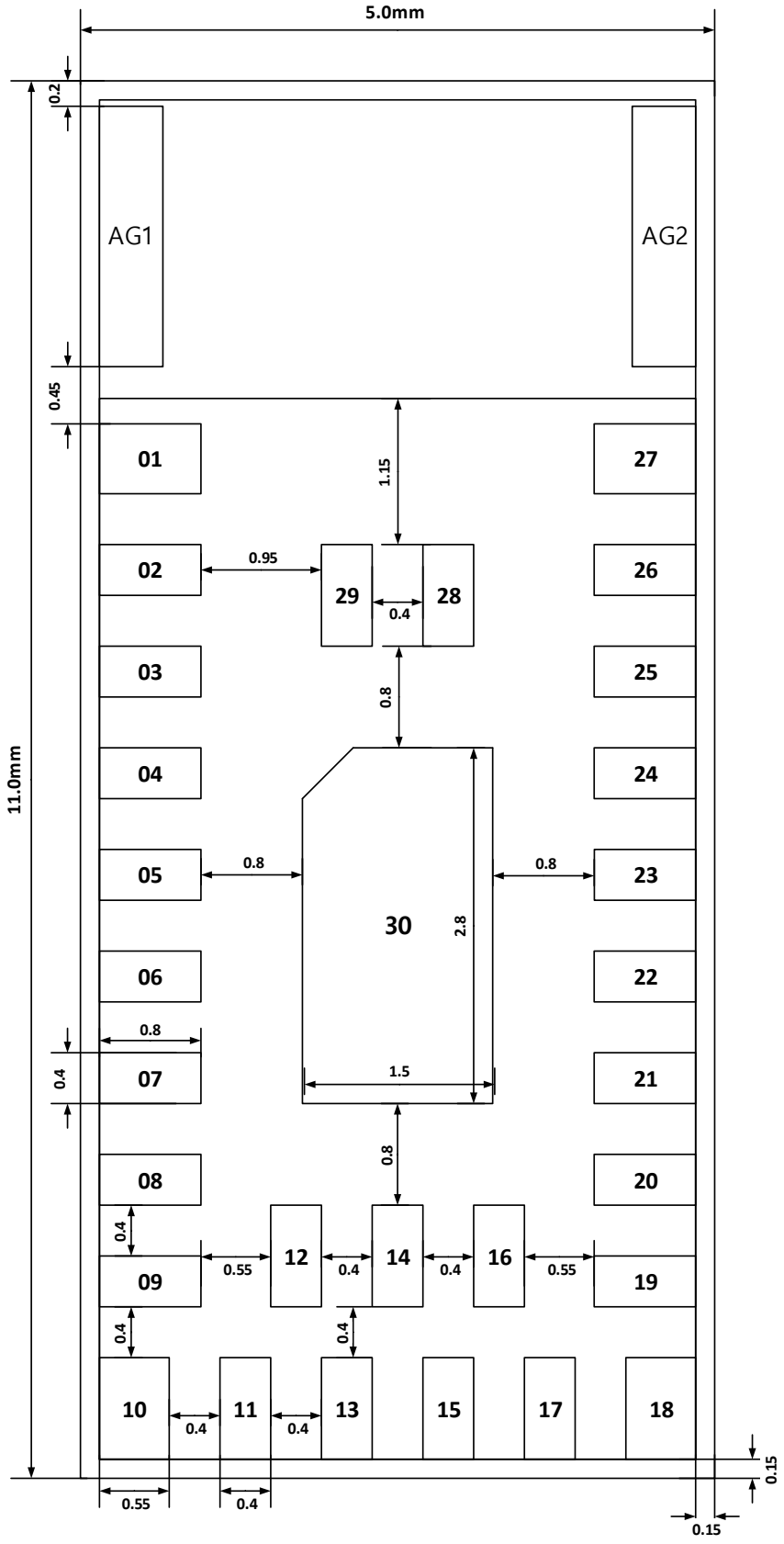


Pin Configuration (TOP VIEW)

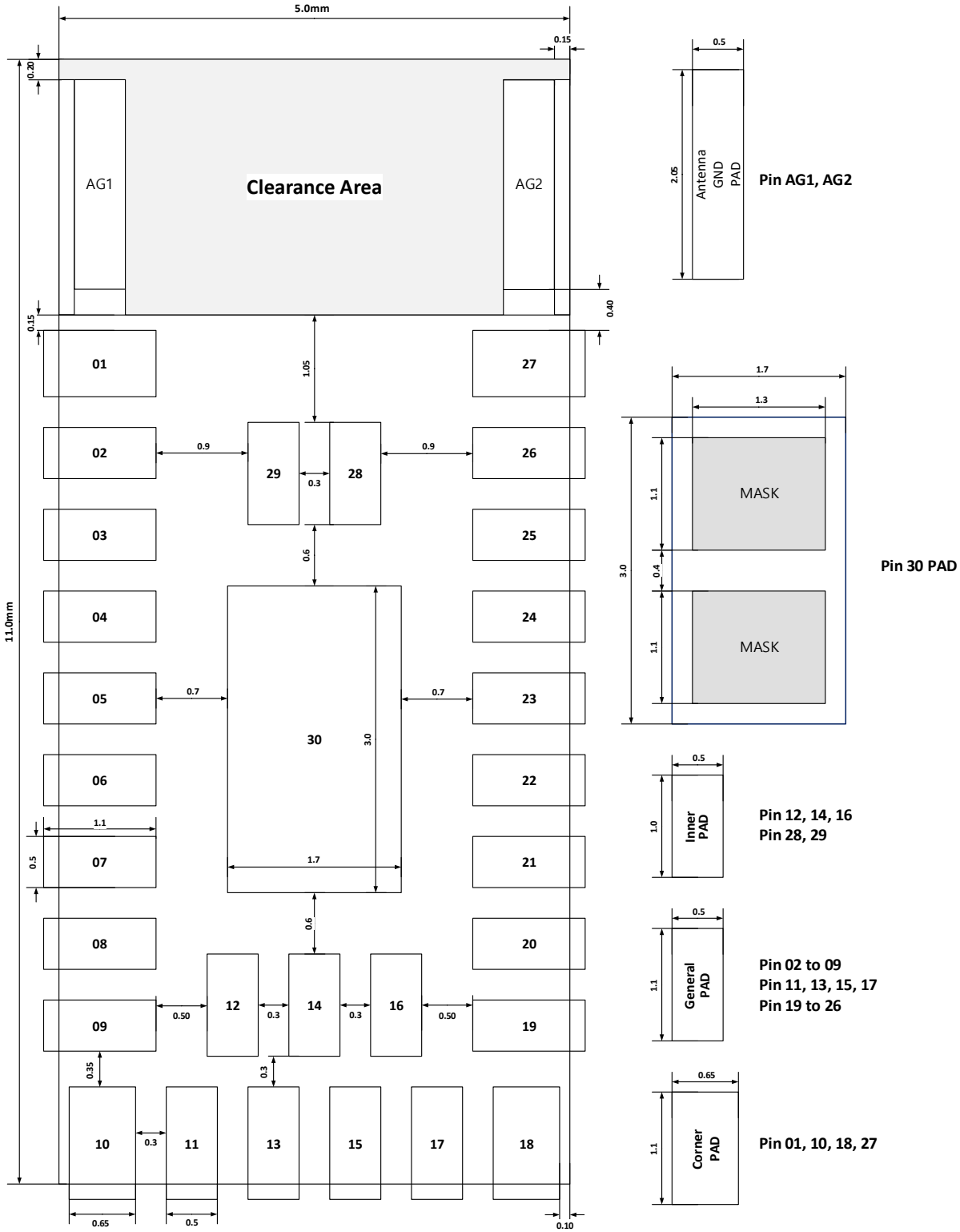
1.5 Device Terminal Functions

Pin No.	Pin Name	Pin Function	Description	NOTE	
01	GND	GROUND	Ground Pin.		
02	INT_ANT	INTERNAL ANTENNA IN / OUT	Internal antenna. It should be connected to Pin 02 RF for normal operation.		
03	RF	RF IN / OUT PORT	Bluetooth 50Ω transmitter output / receiver input		
04	GND	GROUND	Ground Pin.		
05	SWDIO	DIGITAL I/O	Serial Wire Debug I/O for debug and programming		
06	SWDCLK	DIGITAL INPUT	Serial Wire Debug clock input for debug and programming		
07	P0.21	DIGITAL I/O	General purpose I/O pin.		
	nRESET	nRESET	Configurable as system RESET pin.		
08	P0.12	DIGITAL I/O	General purpose I/O pin.	▣ AT communication Factory Reset & Disconnecting	■ More than 4s HIGH : Factory Reset ■ Rising Edge(HIGH) : Disconnected
09	GND	GROUND	Ground Pin.		
10	GND	GROUND	Ground Pin.		
11	P0.08	DIGITAL I/O	General purpose I/O pin.		
	RXD	DIGITAL INPUT	UART RXD		
12	P0.04	DIGITAL I/O	General purpose I/O pin.	▣ AT communication Enter Sleep / Wakeup	■ Rising Edge(HIGH) : Sleep Mode ■ Falling Edge(LOW) : Wakeup
	AIN2	ANALOG INPUT	SAADC/COMP/LPCOMP input		
13	P0.06	DIGITAL I/O	General purpose I/O pin.		
	TXD	DIGITAL OUTPUT	UART TXD		
14	P0.03	DIGITAL I/O	General purpose I/O pin.	▣ AT communication Connection Status	■ Connected : High ■ Disconnected : Low
	AIN1	ANALOG INPUT	SAADC/COMP/LPCOMP input		
15	P0.07	DIGITAL I/O	General purpose I/O pin.		
	CTS	DIGITAL OUTPUT	UART CTS		
16	P0.02	DIGITAL I/O	General purpose I/O pin.	▣ AT communication AT Command / BYPASS	■ AT Command Mode : High ■ BYPASS Mode : Low
	AIN0	Analog input	SAADC/COMP/LPCOMP input		
17	P0.05	DIGITAL I/O	General purpose I/O pin.		
	RTS	DIGITAL INPUT	UART RTS		
18	GND	GROUND	Ground Pin.		
19	P0.00	DIGITAL I/O	General purpose I/O pin.		
	XL1	ANALOG INPUT	Connection for 32.768 kHz crystal (LFXO)		
20	P0.01	DIGITAL I/O	General purpose I/O pin.		
	XL2	ANALOG INPUT	Connection for 32.768 kHz crystal (LFXO)		
21	VDD	POWER	Power supply pin.		
22	DEC4	POWER	1.3 V regulator supply decoupling Input from DC/DC converter. Output from 1.3 V LDO		
23	DCC	POWER	DC/DC regulator output		
24	P0.28	DIGITAL I/O	General purpose I/O pin.		
	AIN4	ANALOG INPUT	SAADC/COMP/LPCOMP input		
25	P0.09	DIGITAL I/O	General purpose I/O pin.		
	NFC1	NFC INPUT	NFC antenna connection		
26	P0.10	DIGITAL I/O	General purpose I/O pin.		
	NFC2	NFC INPUT	NFC antenna connection		
27	GND	GROUND	Ground Pin.		
28	P0.18	DIGITAL I/O	General purpose I/O pin.		
	TRACEDATA[0]		Trace port output		
29	P0.20	DIGITAL I/O	General purpose I/O pin.		
	TRACECLK		Trace port clock output		
30	GND	GROUND	Ground Pin.		
AG1	GND	GROUND	Internal antenna Ground 1 Pin.		
AG2	GND	GROUND	Internal antenna Ground 2 Pin.		

1.6 Package Dimensions & Land Pattern



Top view



Land Pattern

2. Characteristics

2.1 Electrical Characteristics

■ Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
VDD		-0.3	+3.9	V
GND			0	V
$V_{I/O}$, VDD≤3.6V		-0.3	VDD + 0.3	V
$V_{I/O}$, VDD >3.6V		-0.3	+3.9	V
Storage temperature		-40	+85	°C
Radio	RF Input Level		10	dBm
MSL	Moisture Sensitivity Level	2		
ESD HBM	Human Body Model		1	kV
ESD MM	Machine Model		100	V
Endurance	Flash Memory Endurance	10000		write/erase cycles
Retention	Flash Memory Retention	10 years		At 40 °C

■ Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD	LDO Regulator Operation (Default Mode)	1.7	3.0	3.6	V
VDD	DC/DC Regulator Oprtation	2.1	3.0	3.6	V
$t_{R_}$VDD	Supply rise time (0V to 1.7V)			60	ms
TA	Operation temperature	-40	25	85	°C

■ DC Characteristics

- The Specification applies for Temperature: 25°C, VDD = 3.0V

Symbol	Parameter (condition)	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage	0.7 X VDD		VDD	V
V_{IL}	Input low voltage	VSS		0.3 X VDD	V
$V_{OH,SD}$	Output high voltage, standard drive, 0.5 mA, VDD ≥1.7	VDD-0.4		VDD	V
$V_{OH,HDH}$	Output high voltage, high drive, 5 mA, VDD ≥ 2.7 V	VDD-0.4		VDD	V
$V_{OH,HDL}$	Output high voltage, high drive, 3 mA, VDD ≥ 1.7 V	VDD-0.4		VDD	V
$V_{OL,SD}$	Output low voltage, standard drive, 0.5 mA, VDD ≥1.7	VSS		VSS +0.4	V
$V_{OL,HDH}$	Output low voltage, high drive, 5 mA, VDD ≥ 2.7 V	VSS		VSS +0.4	V
$V_{OL,HDL}$	Output low voltage, high drive, 3 mA, VDD ≥ 1.7 V	VSS		VSS +0.4	V
R_{PU}	Pull-up resistance	11	13	16	kΩ
R_{PD}	Pull-down resistance	11	13	16	kΩ
I_{TX},+4dBm,DCDC	TX only run current (DCDC, 3V) P_{RF}=+4 dBm		7.5		mA
I_{TX},+4dBm	TX only run current P_{RF}=+4 dBm		16.6		mA
I_{RX},1M,DCDC	RX only run current (DCDC, 3V) 1Msps		5.4		mA
I_{RX},1M	RX only run current 1Msps		11.7		mA
I_{OFF}	System OFF current, no RAM retention		0.3		uA
I_{ON}	System ON base current, no RAM retention		1.2		uA
I_{RAM}	Additional RAM retention current per 4 KB RAM section		20		nA

2.2 RF Characteristics

Symbol	Description	Min.	Typ.	Max.	Units
f_{OP}	Operating frequencies	2402		2480	MHz
$f_{PLL,PROG,RES}$	PLL programming resolution		2		kHz
$f_{PLL,CH,SP}$	PLL channel spacing		1		MHz
$f_{DELTA,BLE,1M}$	Frequency deviation @ BLE 1Msps		±250		kHz
P_{RF}	Maximum output power		0	4	dBm
P_{RFC}	RF power control range		24		dB
P_{RFCR}	RF power accuracy			±4	dB
$P_{RF1,1}$	1st Adjacent Channel Transmit Power 1 MHz (1 Msps)		-25		dBc
$P_{RF1,2}$	2nd Adjacent Channel Transmit Power 2 MHz (1 Msps)		-50		dBc
$P_{RX,MAX}$	Maximum received signal strength at < 0.1% PER		0		dBm
P_{SENS}	Sensitivity, 1Msps BLE ideal transmitter, <=37 bytes BER=1E-3[17]		-96		dBm
$RSSI_{ACC}$	RSSI Accuracy Valid range -90 to -20 dBm		±2		dB
$RSSI_{RESOLUTION}$	RSSI resolution		1		dB
$RSSI_{PERIOD}$	Sample period		8		us

3. Terminal Description

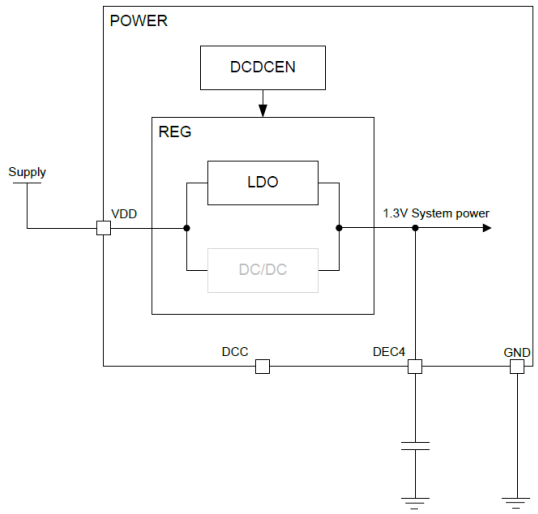
3.1 Regulator

The following internal power regulator alternatives are supported:

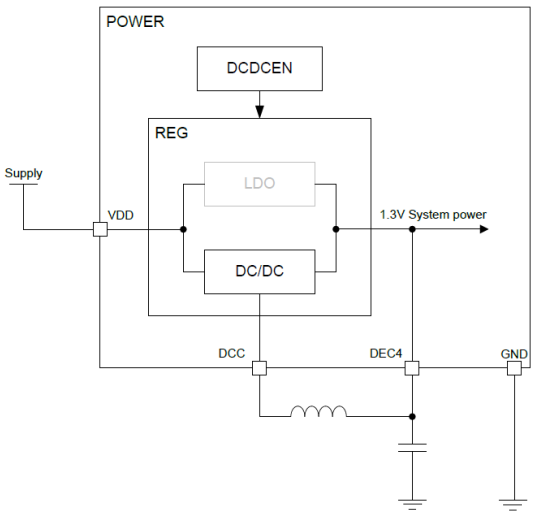
- Internal LDO regulator
- Internal DC/DC regulator

The LDO is the default regulator.

Using the DC/DC regulator will reduce current consumption compared to when using the LDO regulator, but the DC/DC regulator requires an external LC filter to be connected, as shown in Figure.



LDO Regulator Setup



DC/DC Regulator Setup

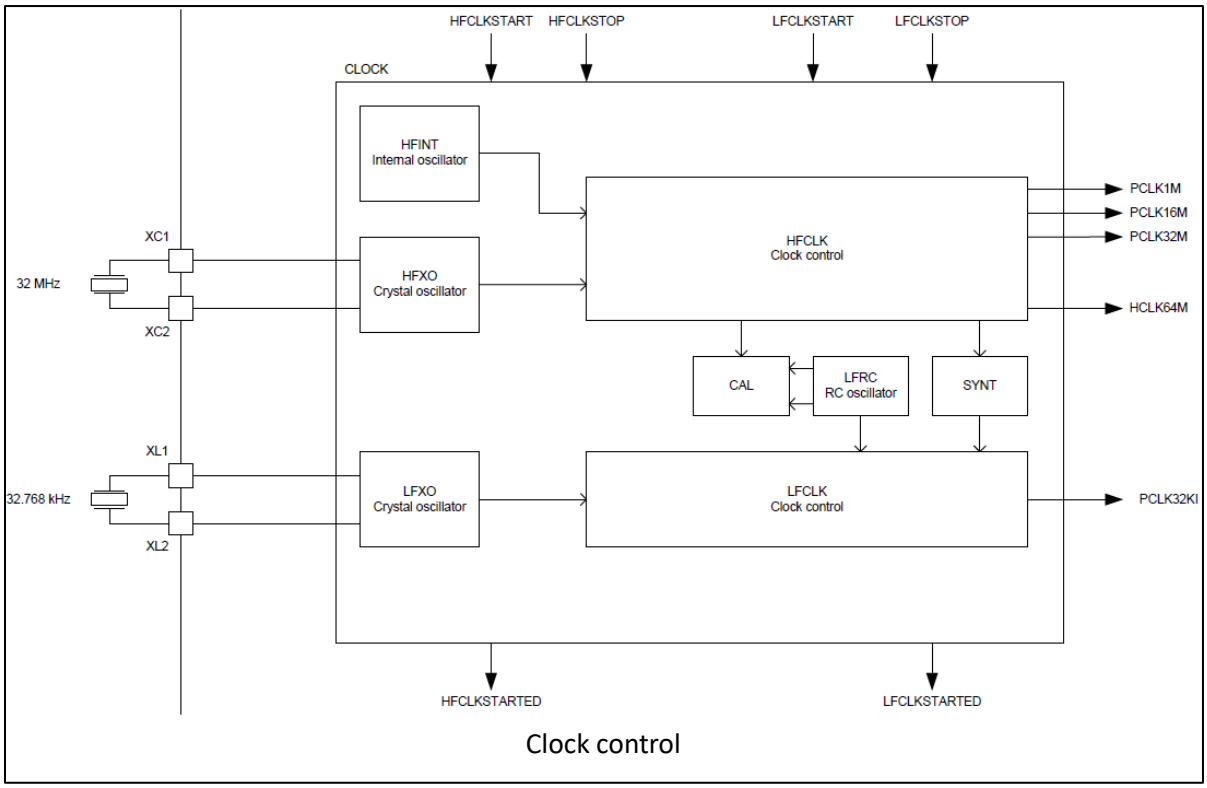
3.2 32.768KHz Crystal Oscillator

The BoT-nLE522 external 32.768KHz Crystal does not required for BLE mode

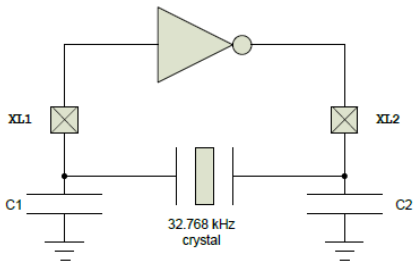
If you choose to use an internal 32.768kHz oscillator, an average of 10uA of current is consumed compared to an external crystal.

The ANT specification requires ± 50ppm accuracy for a 32.768kHz clock. The internal 32.768kHz oscillator may not meet specifications.

BoT-nLE522 F/W does not yet support ANT Mode.



Clock control



Circuit diagram of the 32.768 kHz crystal oscillator

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C_{pcb1} + C_{pin}$$
$$C2' = C2 + C_{pcb2} + C_{pin}$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. Cpcb1 and Cpcb2 are stray capacitances on the PCB.

■ 32.768 kHz RC oscillator (LFRC)

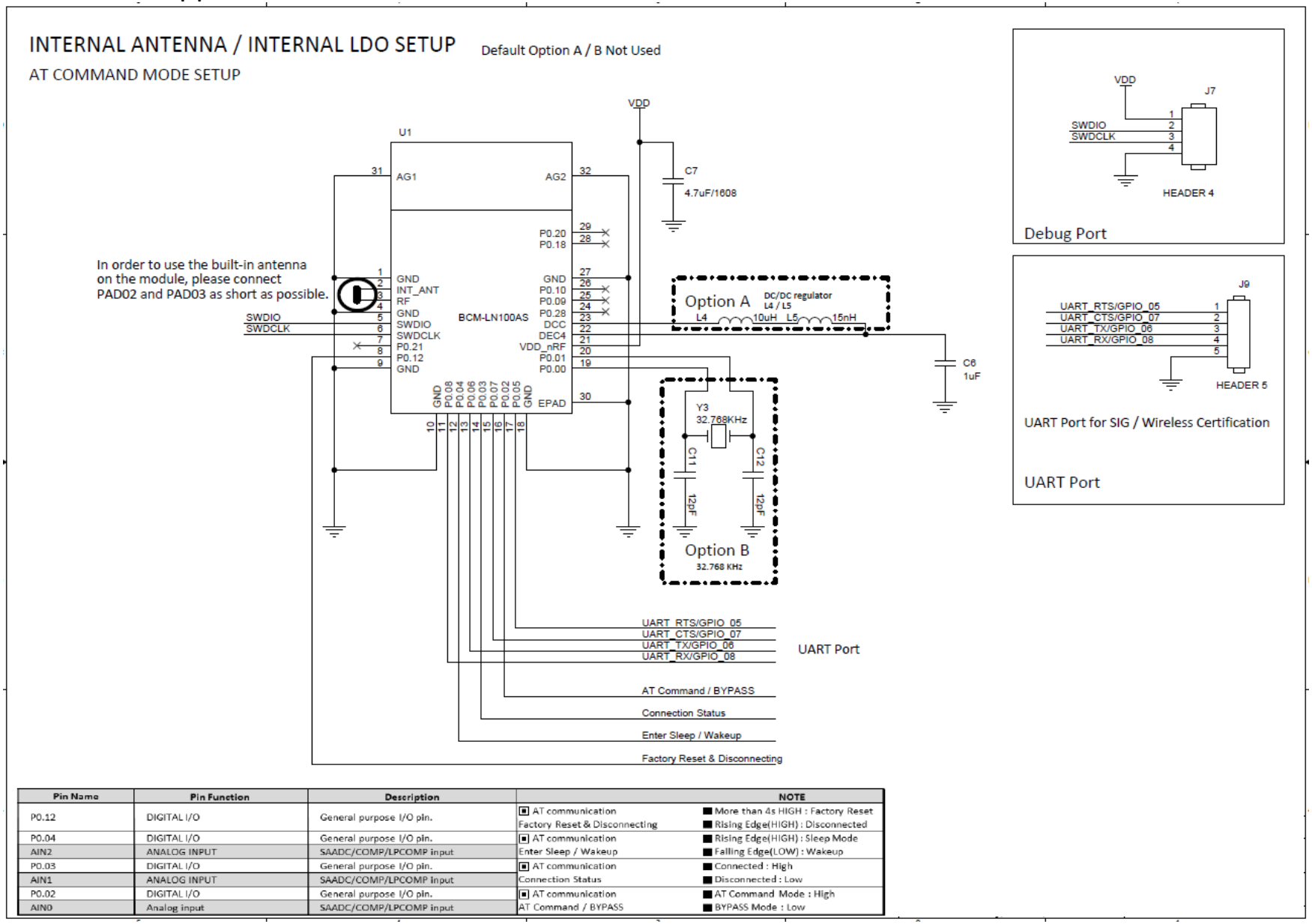
Symbol	Description	Min.	Typ.	Max.	Units
f_{NOM_LFRC}	Nominal frequency		32.768		kHz
f_{TOL_LFRC}	Frequency tolerance		±2		%
$f_{TOL_CAL_LFRC}$	Frequency tolerance for LFRC after calibration		±250		ppm

■ 32.768 kHz crystal oscillator (LFXO)

Symbol	Description	Min.	Typ.	Max.	Units
f_{NOM_LFXO}	Crystal frequency		32.768		kHz
$f_{TOL_LFXO_BLE}$	Frequency tolerance requirement for BLE stack		±250		ppm
$f_{TOL_LFXO_ANT}$	Frequency tolerance requirement for ANT stack		±50		ppm
C_{L_LFXO}	Load capacitance			12.5	pF
C_{0_LFXO}	Shunt capacitance			2	pF
R_{S_LFXO}	Equivalent series resistance			100	
P_{D_LFXO}	Drive level			1	
C_{pin}	Input capacitance on XL1 and XL2 pads		4		

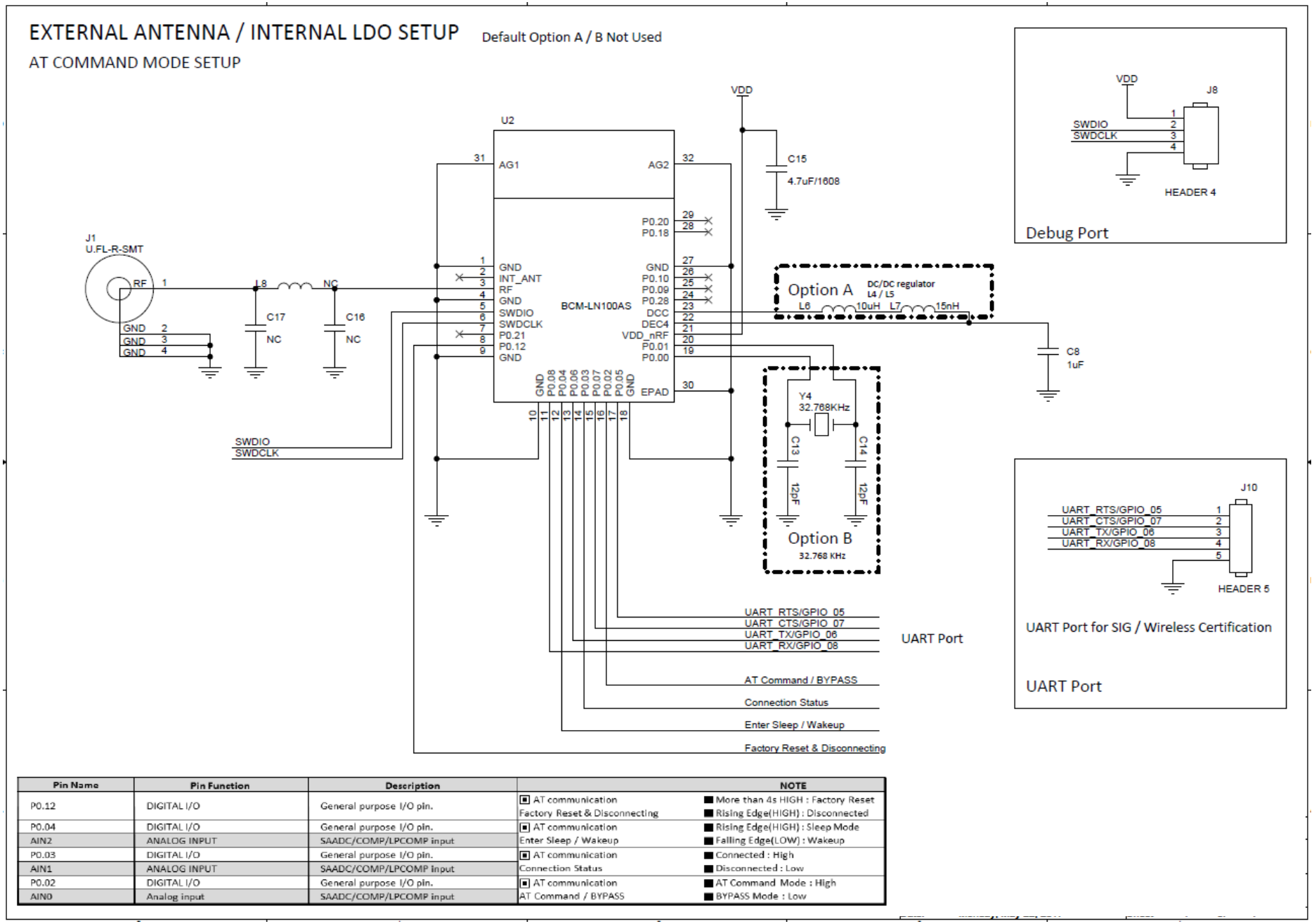
4. Application Schematic

4.1 Internal Antenna Application Schematic



Pin Name	Pin Function	Description	NOTE	
P0.12	DIGITAL I/O	General purpose I/O pin.	▣ AT communication Factory Reset & Disconnecting	■ More than 4s HIGH : Factory Reset ■ Rising Edge(HIGH) : Disconnected
P0.04	DIGITAL I/O	General purpose I/O pin.	▣ AT communication	■ Rising Edge(HIGH) : Sleep Mode
AIN2	ANALOG INPUT	SAADC/COMP/LPCOMP input	Enter Sleep / Wakeup	■ Falling Edge(LOW) : Wakeup
P0.03	DIGITAL I/O	General purpose I/O pin.	▣ AT communication	■ Connected : High
AIN1	ANALOG INPUT	SAADC/COMP/LPCOMP input	Connection Status	■ Disconnected : Low
P0.02	DIGITAL I/O	General purpose I/O pin.	▣ AT communication	■ AT Command Mode : High
AIN0	Analog input	SAADC/COMP/LPCOMP input	AT Command / BYPASS	■ BYPASS Mode : Low

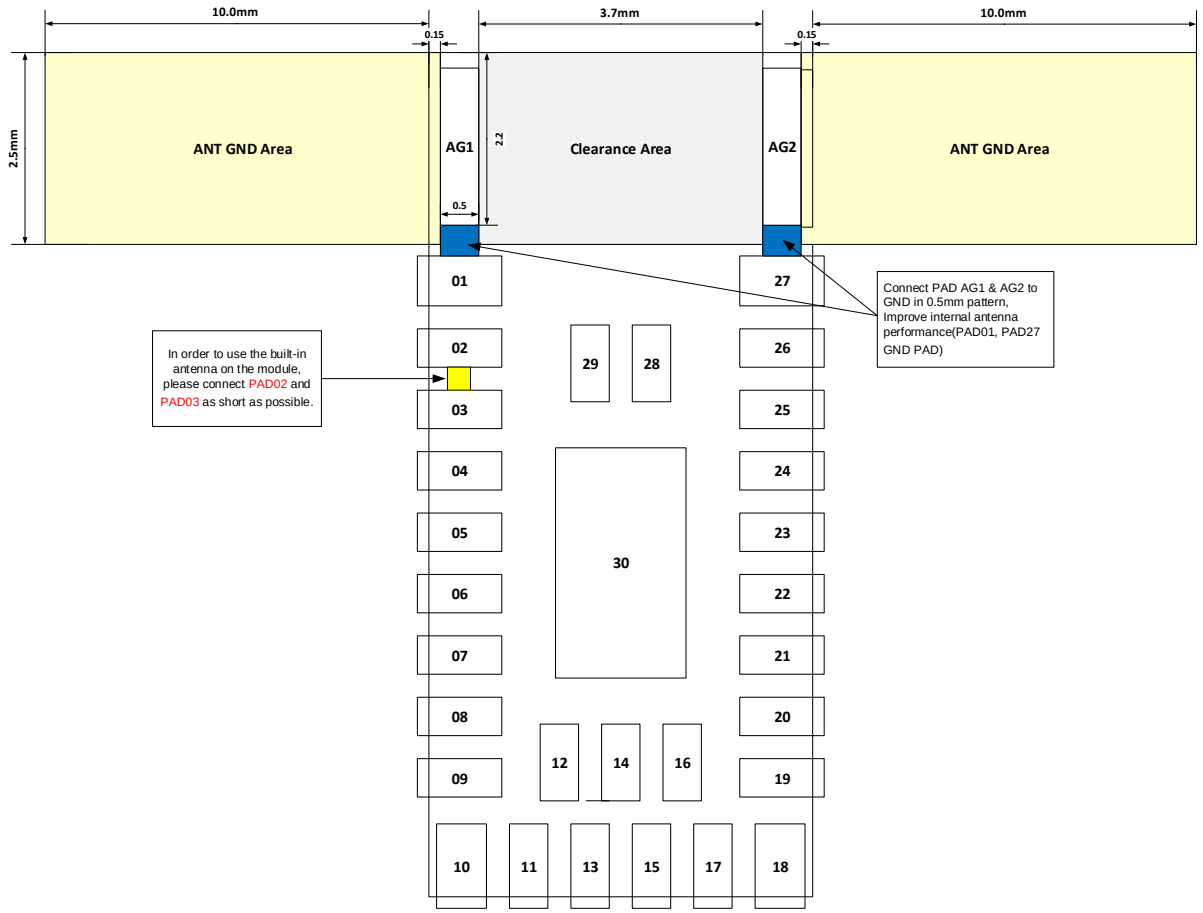
4.2 External Antenna Application Schematic



Pin Name	Pin Function	Description	NOTE	
P0.12	DIGITAL I/O	General purpose I/O pin.	▣ AT communication Factory Reset & Disconnecting	■ More than 4s HIGH : Factory Reset ■ Rising Edge(HIGH) : Disconnected
P0.04	DIGITAL I/O	General purpose I/O pin.	▣ AT communication Enter Sleep / Wakeup	■ Rising Edge(HIGH) : Sleep Mode ■ Falling Edge(LOW) : Wakeup
AIN2	ANALOG INPUT	SAADC/COMP/LPCOMP input		
P0.03	DIGITAL I/O	General purpose I/O pin.	▣ AT communication Connection Status	■ Connected : High ■ Disconnected : Low
AIN1	ANALOG INPUT	SAADC/COMP/LPCOMP input		
P0.02	DIGITAL I/O	General purpose I/O pin.	▣ AT communication AT Command / BYPASS	■ AT Command Mode : High ■ BYPASS Mode : Low
AIN0	Analog input	SAADC/COMP/LPCOMP input		

5. Layout Guide

5.1 Internal Antenna Design Guide

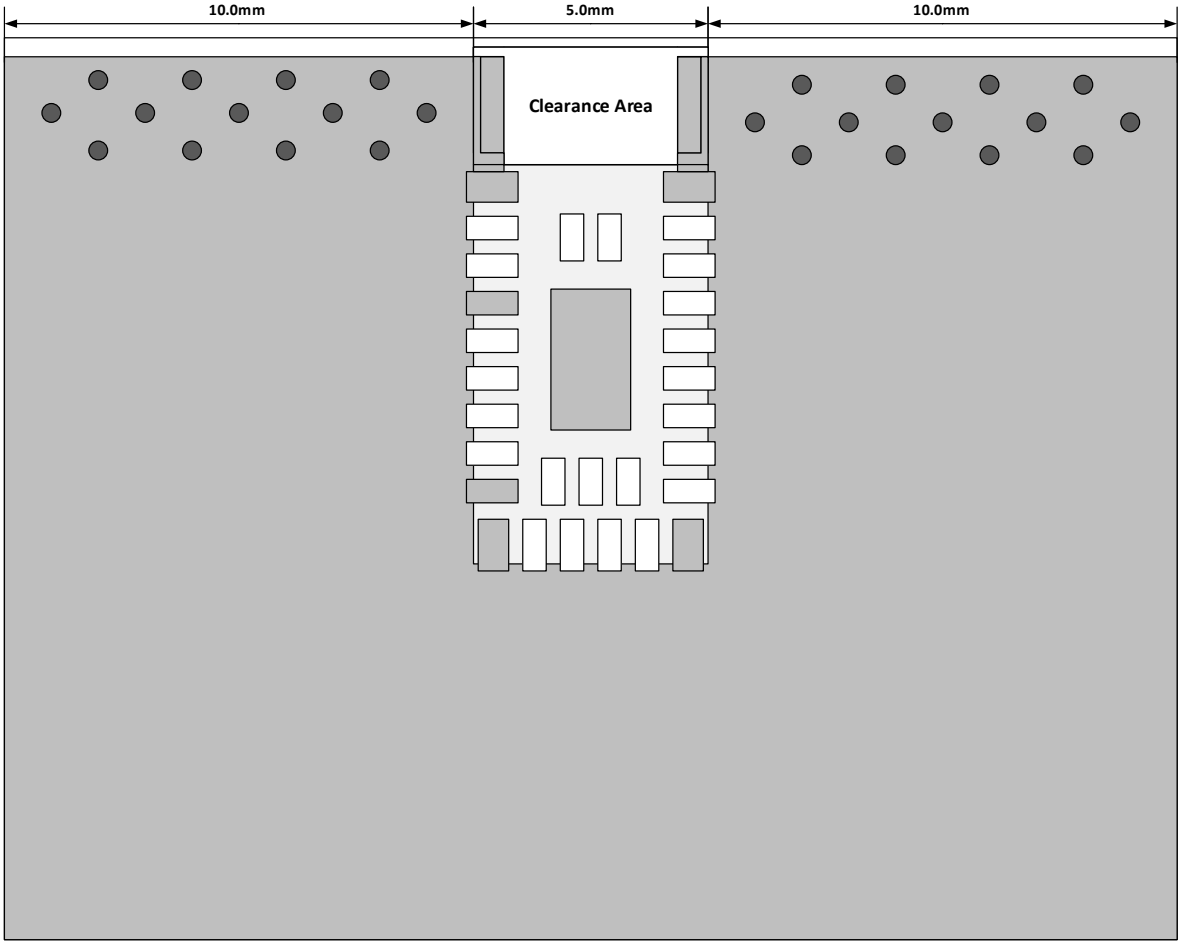


5.2 Internal Antenna Layout Guide

To achieve best radio performance for BoT-nLE522, It is recommended to use the module at the edge of the PCB

Do not place metal, trace, via, or parts in the Antenna Clearance Area.

AG1, AG2 pins must be connected to GND with flood over. Place the GND vias as close to the GND pins as possible.



6. Reflow Temperature Profile

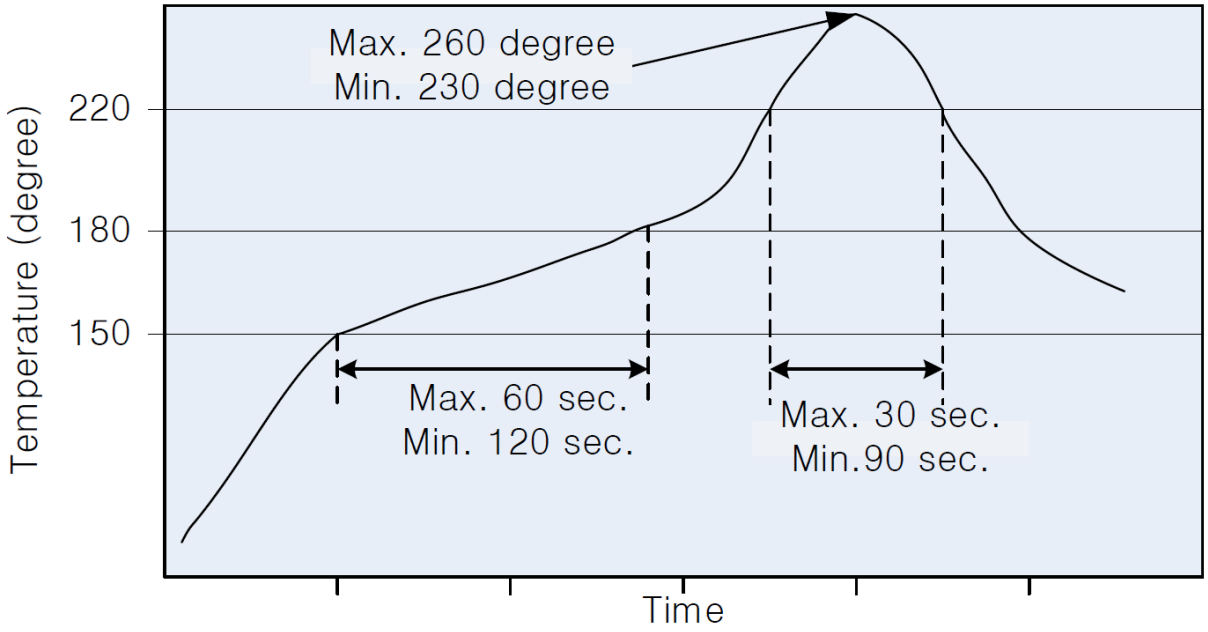
Recommended solder reflow profile are shown in below and follow the lead-free profile I accordance with JEDEC Std 20C.

Table lists the critical reflow temperatures.

Flux residue remaining from board assembly can contribute to lectrochemical migration over time.

This depends on number of factors, including flux type, amount of flux residue remaining after reflow, and stress conditions during product use, such as temperature, humidity, and potential difference between pins.

Care should be taken in selecting production board/module assembly processes and materials, taking into account these factors.



Process Step	Lead-Free Solder
Ramp rate	3°C/sec
Preheat	Max. 150°C to 180°C, 60 to 180 sec
Time above liquidus	+220°C 30 to 90 sec
Peak temperature	+255°C ±5°C
Time within 5°C of peak temperature	10 to 20 sec
Ramp-down rate	6°C/sec max