BoT-cDA110

DATASHEET

V 1.0.1

CHIPSEN

■ History

Ver	Date	Description	Author
1.0.1	2022. 06. 29	- Feature, Characteristics update	Enoch
1.0.0	2022. 04. 06	- Family model type add. - UART Baud rate change - Pin description and Application schematic update	Enoch
0.1.0	2022. 02. 11	- minimum operating voltage change - RF Characteristic LE update	Enoch
0.0.1	2022. 01. 11	- First release	Enoch

Table of Contents

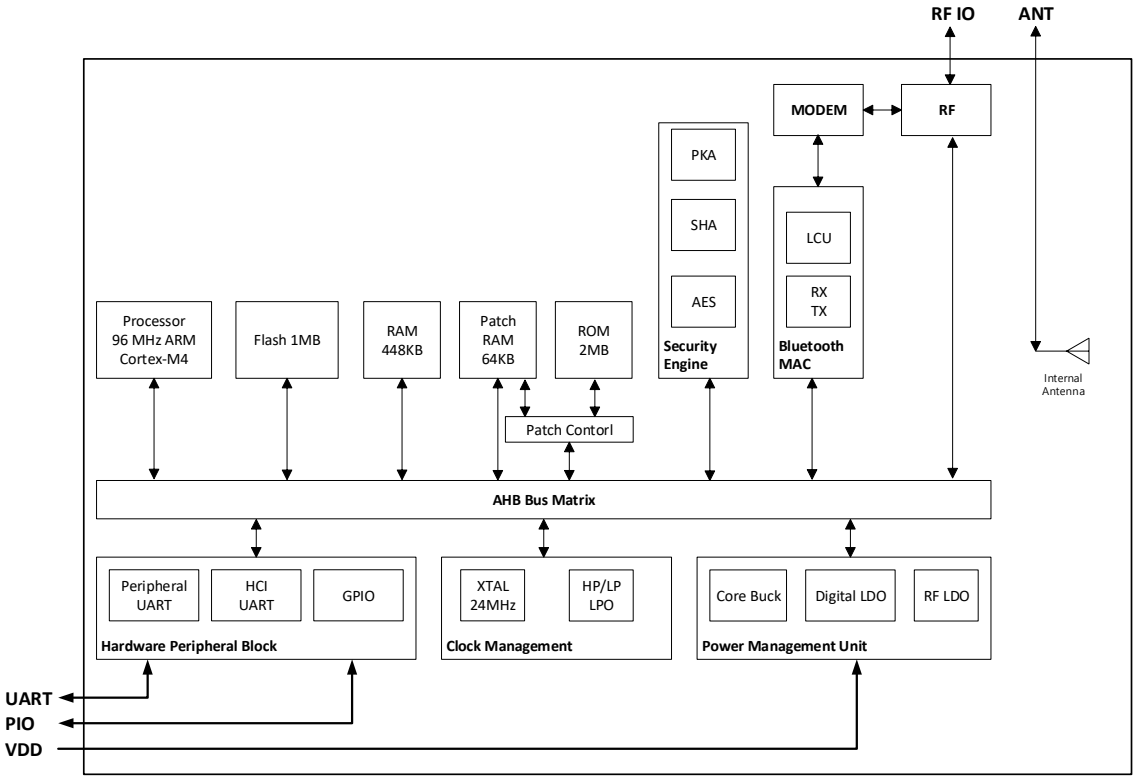
1. General

1.1. Overview

This specification covers Bluetooth module which complies with Bluetooth specification version 5.1 and integrates RF & Baseband controller in small package. This Module has deployed MCU with Bluetooth function included chipset.

All detailed specification including pin outs and electrical specification may be changed without notice.

1.2. Block Diagram



<Block diagram>

1.3. Feature

■ Complies with Bluetooth Core Specification v5.1

■ Supports Basic Rate (BR), Enhanced Data Rate (EDR) 2&3 Mbps

■ TX RF Power” 4dBm

■ RX sensitivity: -91dBm(BR)

■ 96-MHz Arm Cortex-M4 microcontroller unit MCU

■ 1MB Flash, 512KB RAM

■ 1x peripheral UART

■ Hardware security engine

■ 16 GPIOs

■ Wide operating voltage range: 2.7V to 3.6V

■ Operating temperature range (MAX -30℃ ~ 85℃)

■ Competitive Size:

- BoT-cDA110SC, BoT-cDA110SU:14mm x 22mm x 2.4mm: 27Pin

- BoT-cDA110DC, BoT-cDA110DU:15.4mm x 22mm x 6.4mm: 27Pin (with Pin Header)

1.4. Applications

■ Bluetooth data communication

■ Laptop / Handheld Device

■ Bluetooth access point

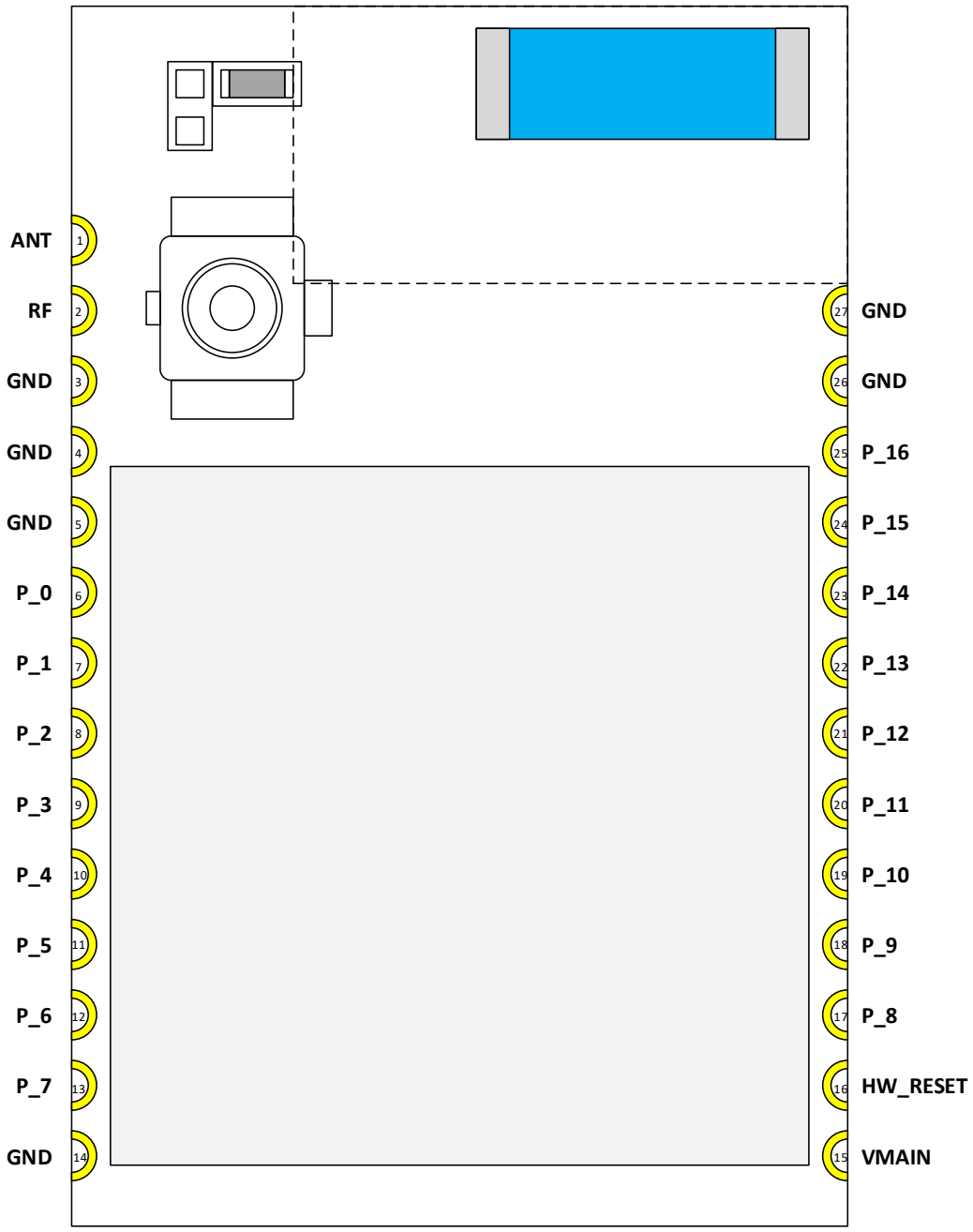
■ Industrial automation

■ Remote meter reading system

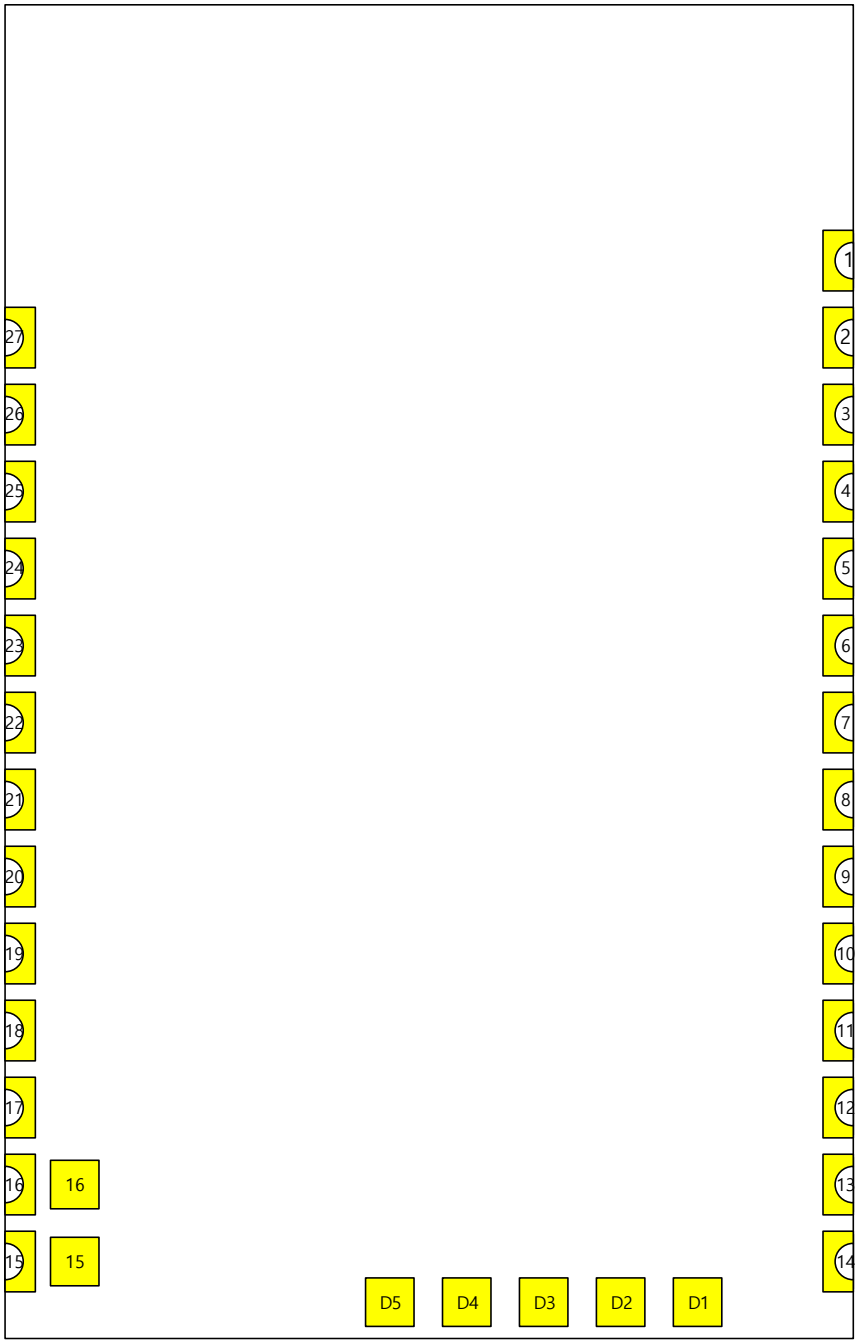
■ POS / Mobile printer

1.5. Pin Configuration

1.5.1. BoT-cDA110SC, BoT-cDA110SU



< Pin configuration (Top view) >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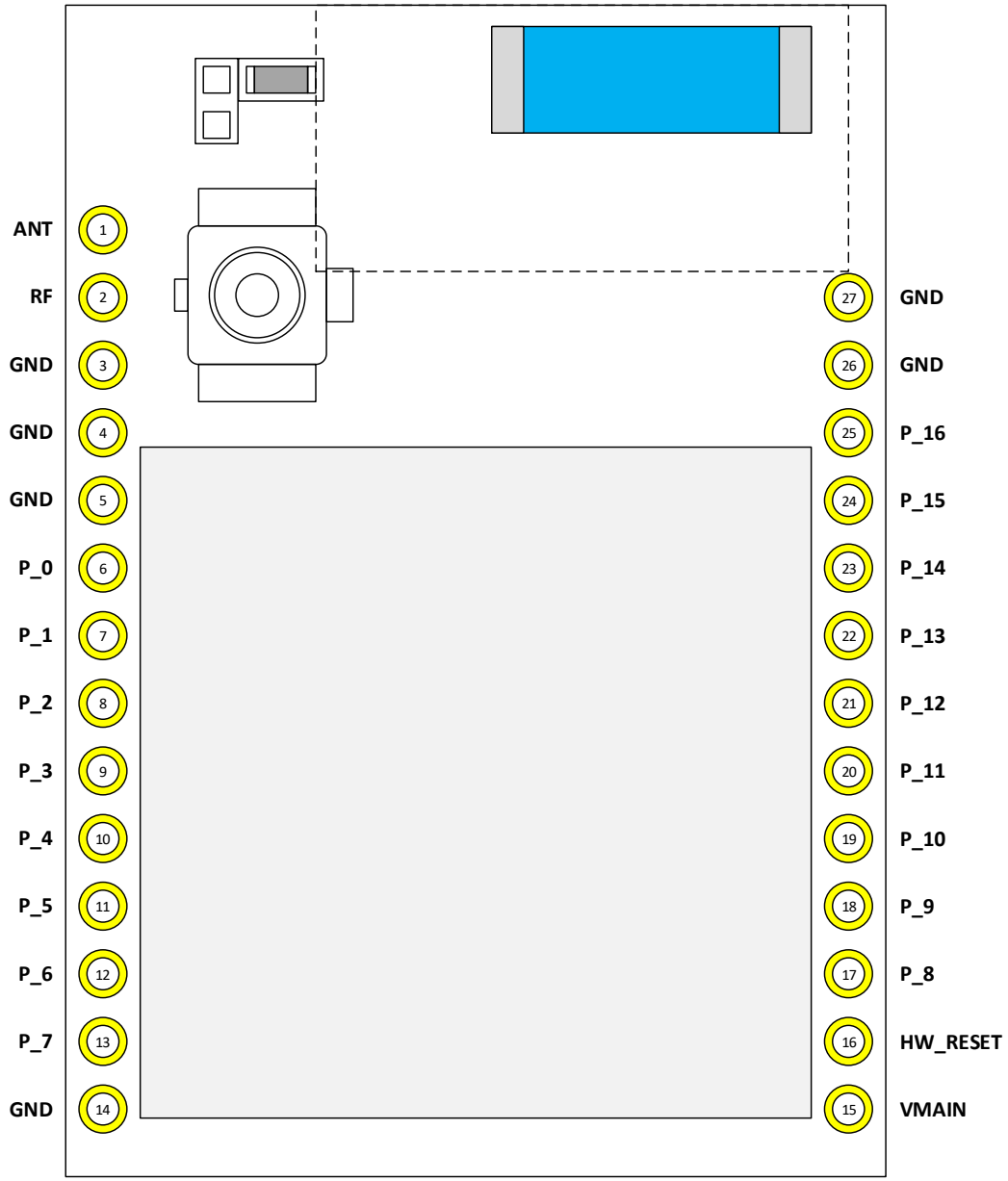
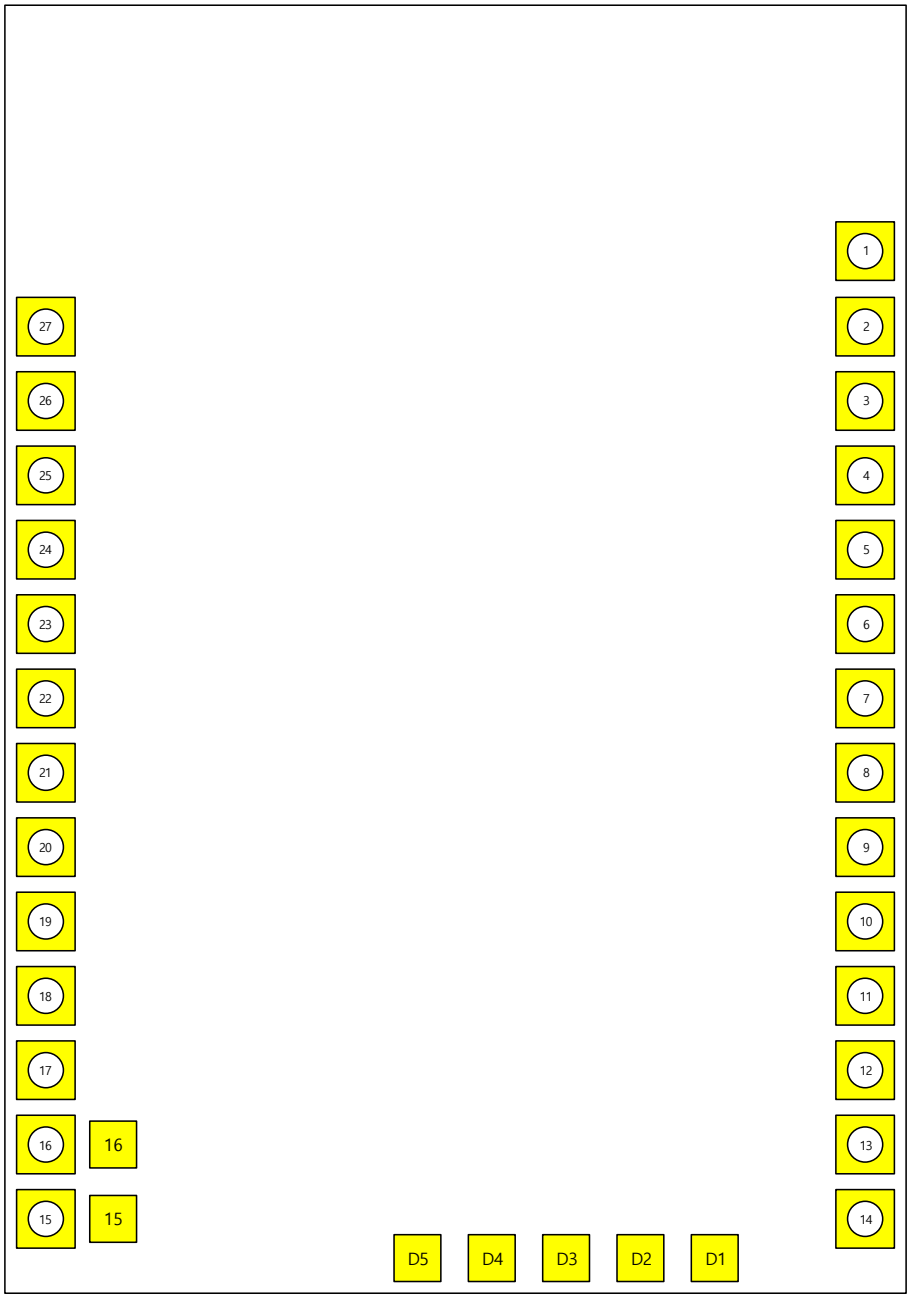
< Bottom View >

1.5.2. BoT-cDA110DC, BoT-cDA110DU



< Pin configuration (Top view) >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1.6. Device Terminal Function

Pin No.	Pin Name	Pin Function	Description
1	ANT	Internal Antenna IN/OUT	Internal antenna. It should be connected to 2 Pin RF for using internal antenna.
2	RF	Radio In/out PORT	Bluetooth 50Ω Tx/Rx Port
6	P_0	Digital I/O	General purpose I/O pin.
7	P_1	Digital I/O	General purpose I/O pin.
8	P_2	Digital I/O	General purpose I/O pin.
9	P_3	Digital I/O	General purpose I/O pin.
10	P_4	Digital I/O	General purpose I/O pin.
	BT DISCONNECT	Digital Input	Disconnect Bluetooth device at detect high edge. [1)] Active High edge detection
11	P_5	Digital I/O	General purpose I/O pin.
	ADC_0 (T.B.D)	ADC Input	Reserve (T.B.D, contact manufacture). [1)]
12	P_6	Digital I/O	General purpose I/O pin.
	ADC_1 (T.B.D)	ADC Input	Reserve (T.B.D, contact manufacture). [1)]
13	P_7	Digital I/O	General purpose I/O pin.
	FACTORY RESET	Digital Input	Set to factory default state after logic high 1 second. [1)] Active High 1 second.
17	P_8	Digital I/O	General purpose I/O pin.
	UART_RXD	Digital Input	UART Receive [1)]
18	P_9	Digital I/O	General purpose I/O pin.
	UART_TXD	Digital output	UART Transmit [1)]
19	P_10	Digital I/O	General purpose I/O pin.
	UART_RTS	Digital output	UART Request to Send [1)]
20	P_11	Digital I/O	General purpose I/O pin.
	UART_CTS	Digital Input	UART Clear to Send [1)]
21	P_12	Digital I/O	General purpose I/O pin.
22	P_13	Digital I/O	General purpose I/O pin.
23	P_14	Digital I/O	General purpose I/O pin.
	BT STATUS	Digital output	BT Status indicator. Connection is logic high. [1),2)]
24	P_15	Digital I/O	General purpose I/O pin.
25	P_16	Digital I/O	General purpose I/O pin.
15	VMAIN	Power	Power supply pin
16	HW_RESET	Hardware reset	Internal 470K ohm pull up resistor RC delay for power-on reset. Active low.[3)]
D1-D5	Reserved	Only manufacture use	Not Connect. Do not tied ground, power, any I/O.
3,4,5,14 26,27	GND	Ground	Ground Pin.

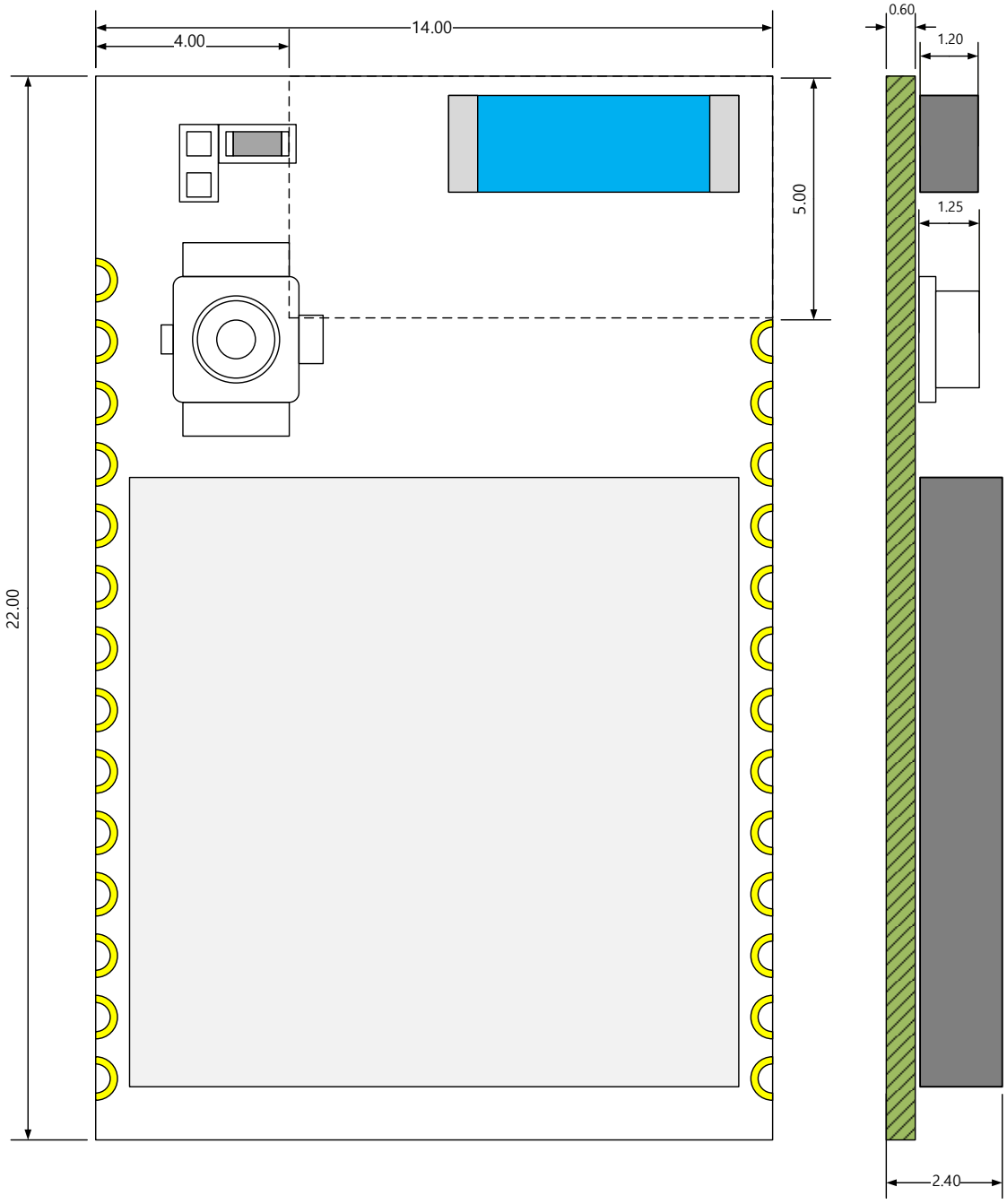
1) This I/O function operate on CHIPSEN commercial firmware.
2) For more information refer to CHIPSEN commercial firmware document.
3) For more information refer to 3.2 EXTERNAL RESET Content

1.7. Dimensions

1.7.1. BoT-cDA110SC, BoT-cDA110SU

■ Unit: mm

■ General Tolerances = ±0.2mm



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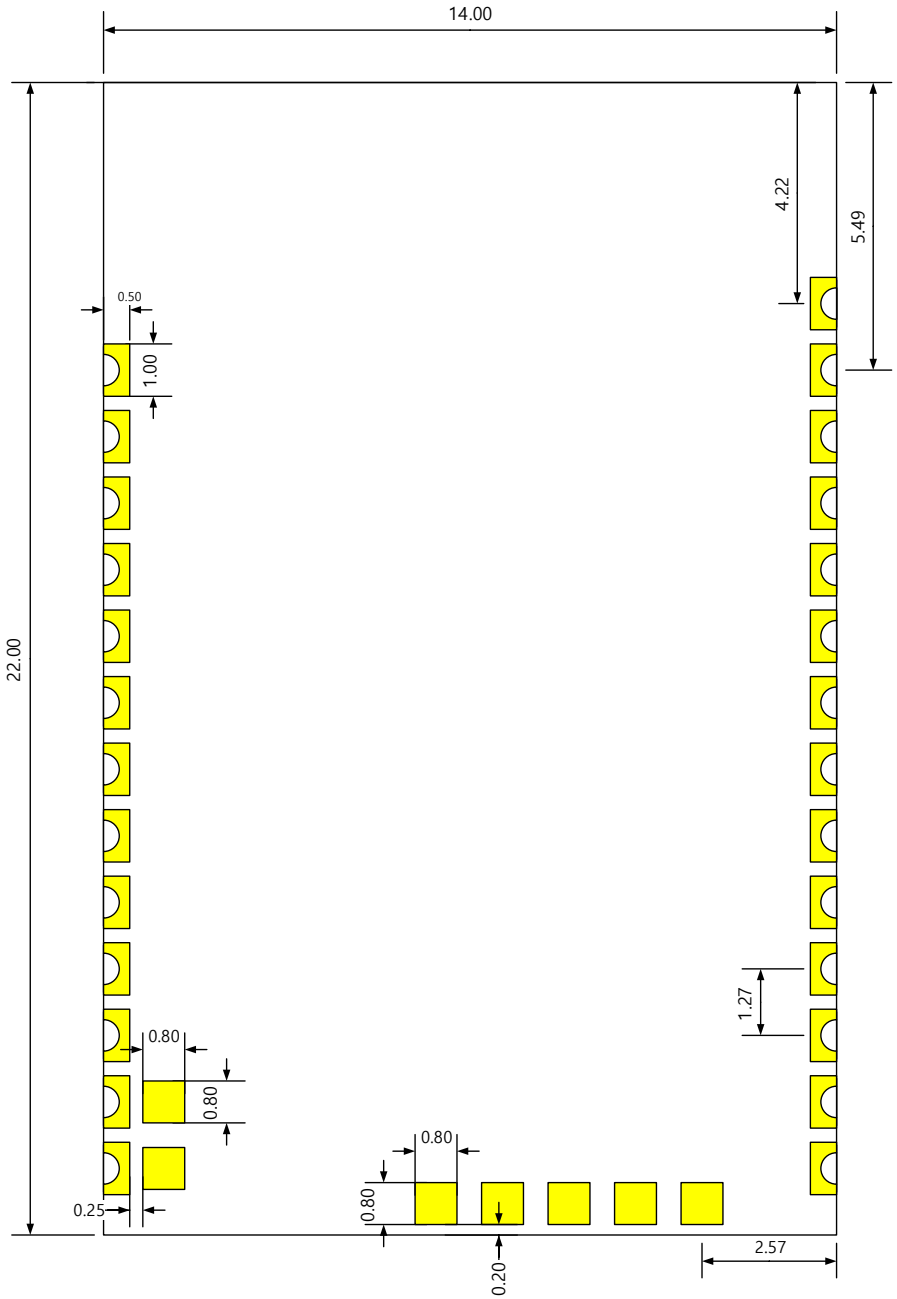

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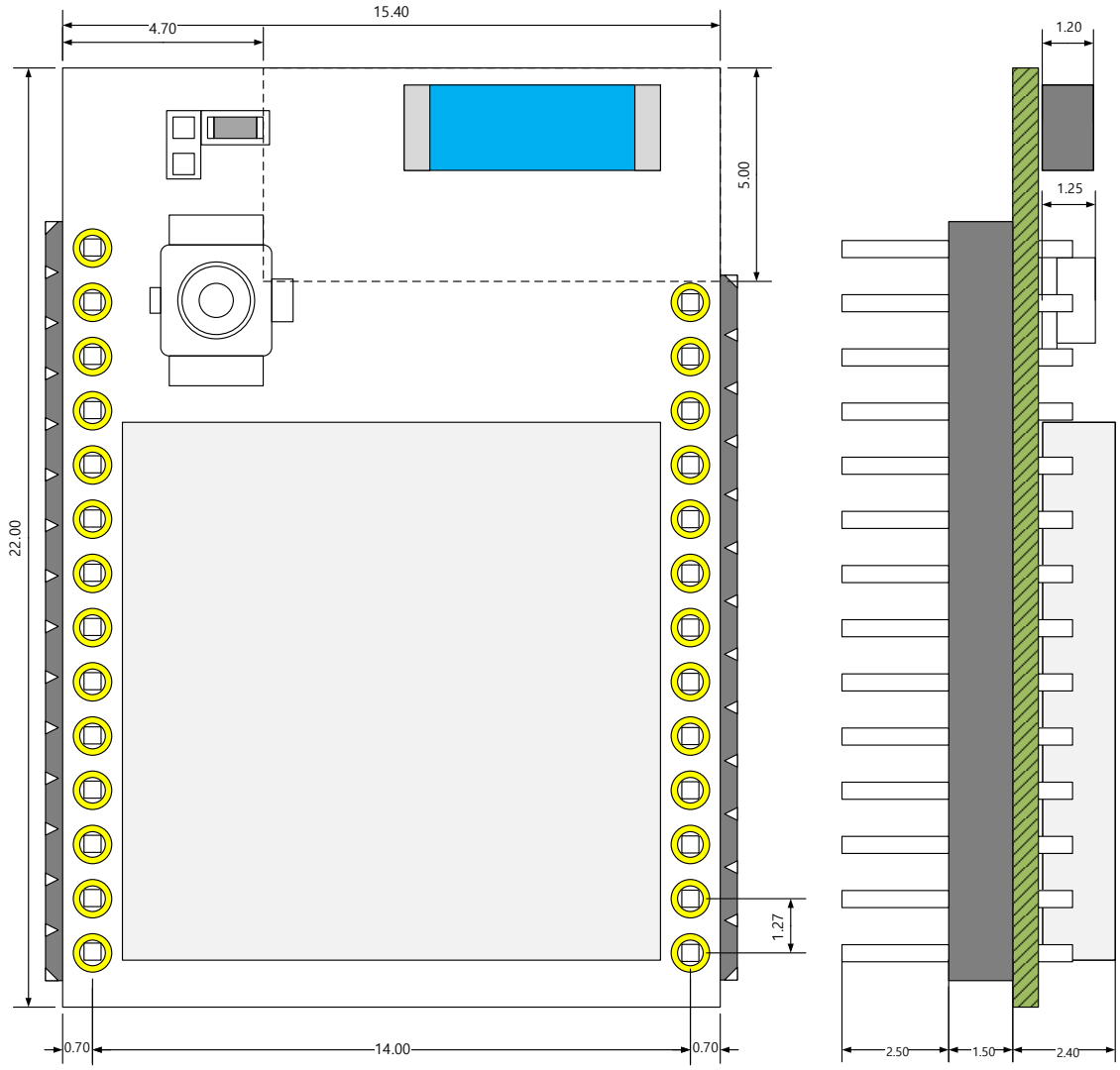
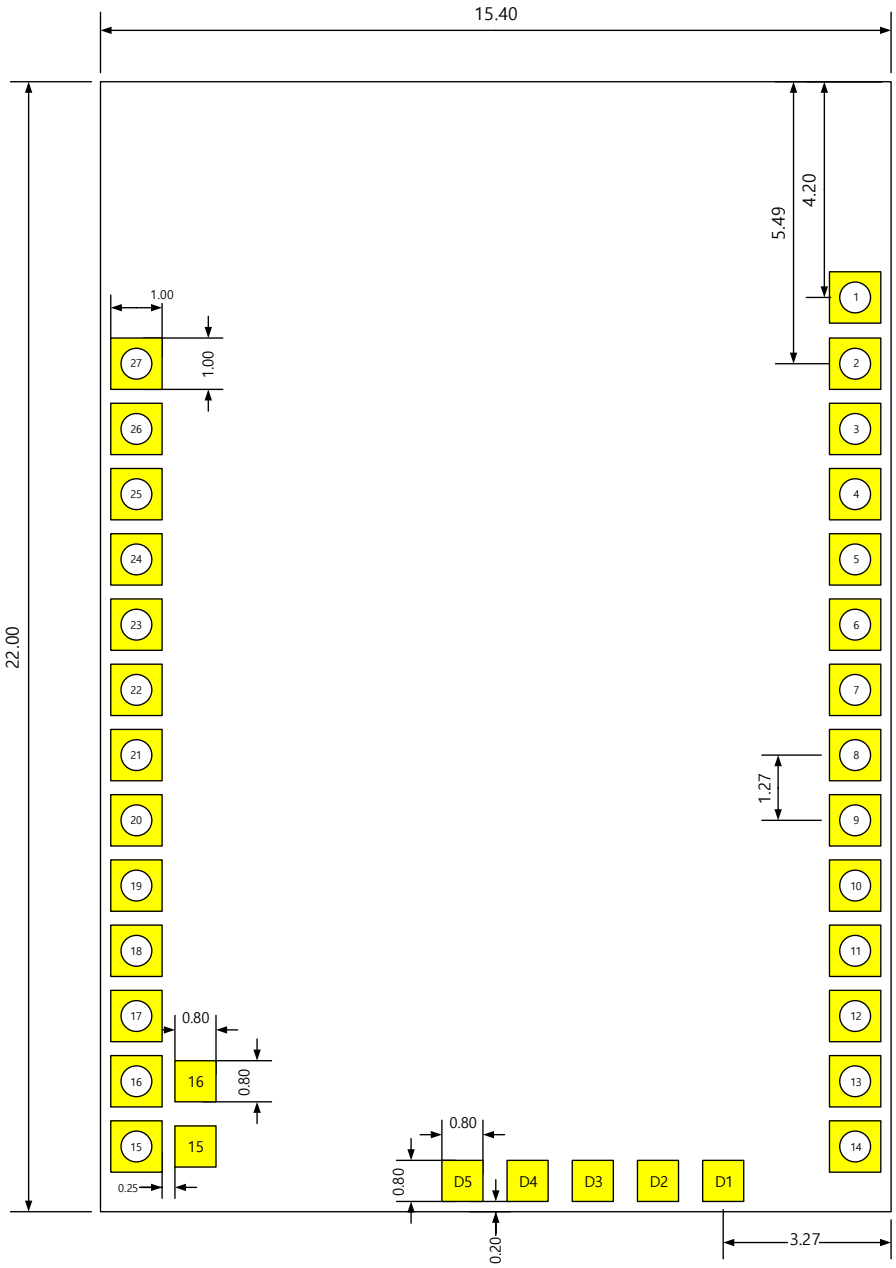
1.7.2. BoT-cDA110DC, BoT-cDA110DU

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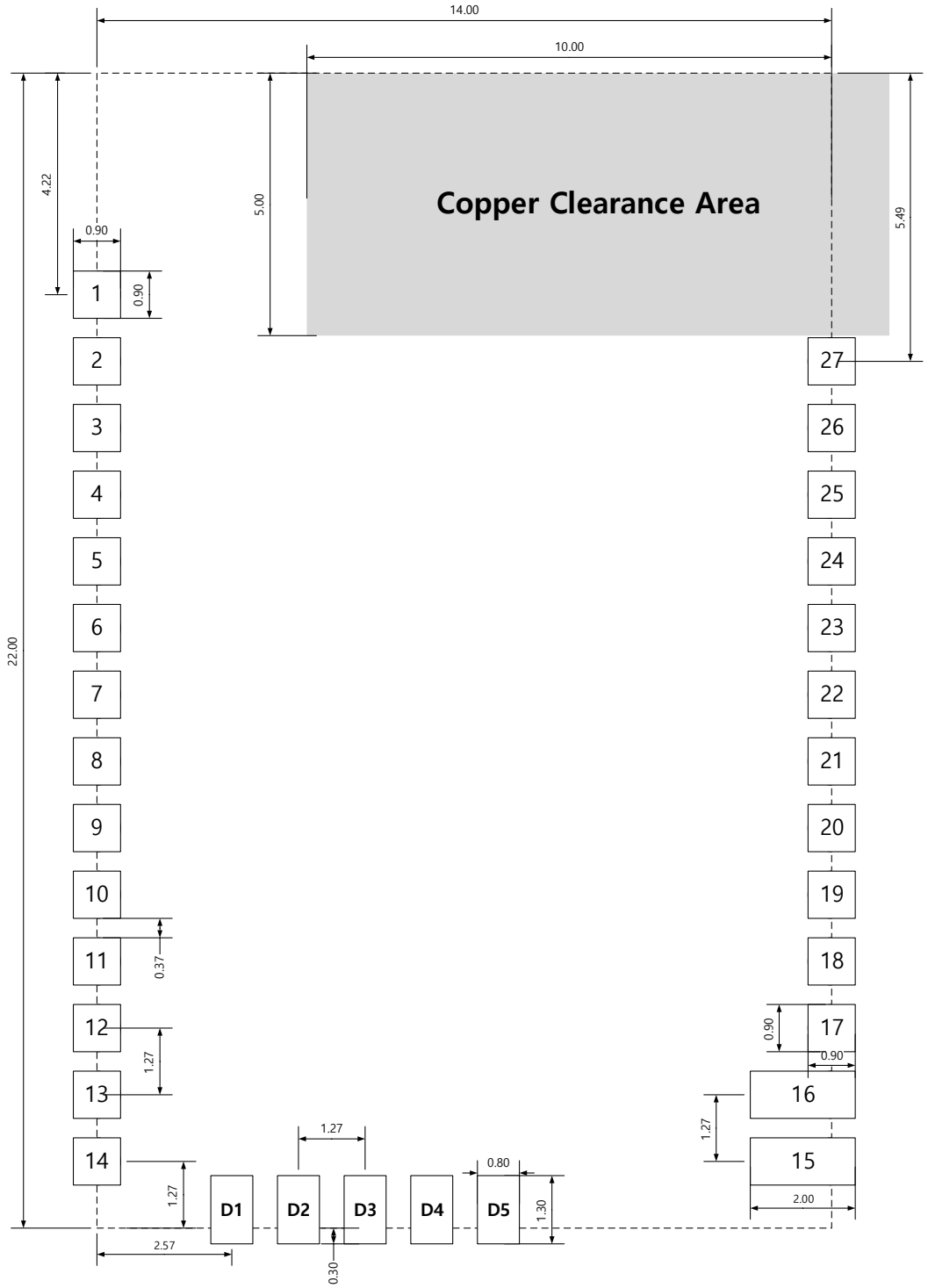
1.8. Land Pattern

■Unit: mm

■ General Tolerances = ±0.2mm



< TOP VIEW >

2. Characteristics

2.1. Electrical Characteristics

■ Absolute Maximum Ratings

ITEM	Min	Typ	Max	Unit
Storage Temperature range	-40	-	150	°C
VMAIN	-	-	3.79	V

■ Recommended Operating Conditions

ITEM	Min	Typ	Max	Unit
Operating Temperature range	-30	20	85	°C
VMAIN	2.7	3	3.6	V

■ Digital I/O Characteristics

ITEM	Min	Typ	Max	Unit
Input low voltage (VMAIN = 3 V)	-	-	0.8	V
Input high voltage (VMAIN = 3 V)	2.4	-	-	V
Output low voltage	-	-	0.45	V
Output high voltage	VMAIN -0.45V	-	-	V

2.2. RF Characteristics (BR/EDR)

RF	Specification	Min	Typ	Max	Unit
Transmit	Frequency range	2402	-	2480	MHz
	Power (@ GFSK)	-	4	-	dBm
	Adjacent Channel Power				
	|M – N| = 2	-	-	-20	dBm
	|M – N| ≥ 3	-	-	-40	dBm
	Out-of-Band Spurious Emission				
	30 MHz to 1 GHz	-	-	-36	dBm
	1.8 GHz to 1.9 GHz	-	-	-47	dBm
	5.15 GHz to 5.3 GHz	-	-	-47	dBm
	Frequency Drift				
	DH1	-25	-	25	KHz
	DH3, DH5	-40	-	40	KHz
	Drift Rate	-20	-	20	KHz/50us
	Modulation Accuracy				
	p/4-DQPSK frequency stability	-10	-	10	KHz
	p/4-DQPSK RMS DEVM	-	-	20	%
	p/4-QPSK Peak DEVM	-	-	35	%
	p/4-DQPSK 99% DEVM	-	-	30	%
	8-DPSK frequency stability	-10	-	10	KHz
	8-DPSK RMS DEVM	-	-	13	%
	8-DPSK Peak DEVM	-	-	25	%
	8-DPSK 99% DEVM	-	-	20	%
	In-Band Spurious Emissions				
	1.0 MHz < |M – N| < 1.5 MHz	-	-	-26	dBm
	1.5 MHz < |M – N| < 2.5 MHz	-	-	-20	dBm
	|M – N| > 2.5 MHz	-	-	-40	dBm
Receiver	**RX sensitivity, Dirty Tx is OFF**				
	GFSK, 0.1% BER, 1 Mbps	-	-91	-	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	-	-93	-	dBm
	8-DPSK, 0.01% BER, 3 Mbps	-	-87	-	dBm

3. Terminal Description

3.1. Power Connection (VMAIN)

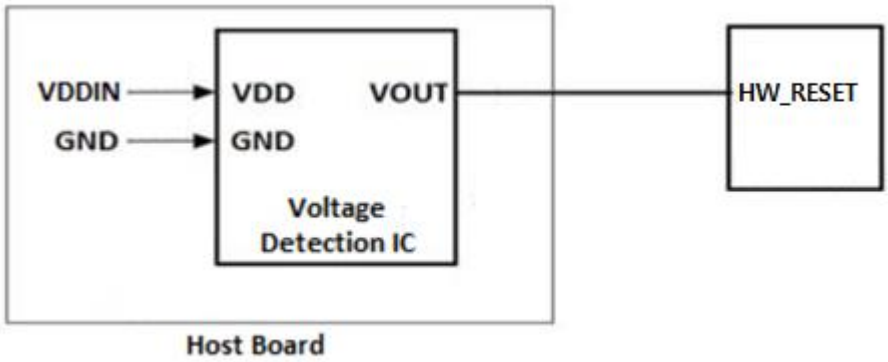
The BoT-cDA110 contains one power supply connection, VDD. VDD accepts a supply input of 2.7 V to 3.6 V. The maximum power supply ripple for this power connection is 100 mV.

Considerations and Optional Components for Brownout (BO) Conditions

Power supply design must be completed to ensure that the BoT-cDA110 module does not encounter a Brownout condition, which can lead to unexpected functionality, or module lock up. A Brownout condition may be met if power supply provided to the module during power up or reset is in the range shown below: VIL ≤ VDD ≤ VIH. Refer to “2.1 Digital IO Characteristics”

System design should ensure that the condition above is not encountered when power is removed from the system. In the event that this cannot be guaranteed (i.e. battery installation, high value power capacitors with slow discharge), it is recommended that an external voltage detection device be used to prevent the Brownout voltage range from occurring during power removal.

Refer to the recommended circuit design when using an external voltage detection IC.



< Reference Circuit Block Diagram for External Voltage Detection IC>

In the event that the module does encounter a Brownout condition, and is operating erratically or not responsive, power cycling the module will correct this issue and once reset, the module should operate correctly. Brownout conditions can potentially cause issues that cannot be corrected, but in general, a power-on-reset operation will correct a Brownout condition.

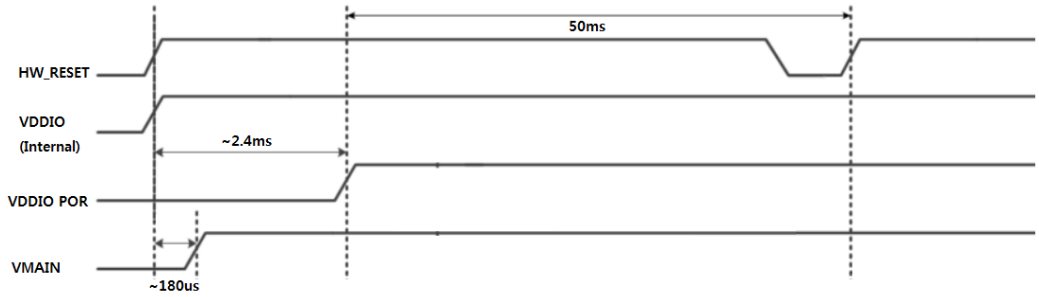
3.2. External Reset (HW_RESET)

The BoT-cDA110 has an integrated power-on reset circuit which completely resets all circuits to a known power-on state. This action can also be invoked by an external reset signal, forcing it into a power-on reset state. HW_RESET is an active-low input signal on the BoT-cDA110 module (solder pad 16). The BoT-cDA110 does not require external pull-up resistors on the HW_RESET input. Refer to Figure “Reset Timing” for HW_RESET operating and timing requirements during power on events. During power on operation, the HW_RESET connection to the BoT-cDA110 is required to be held low 50ms after the VDD power supply input to the module is stable. This can be accomplished in the following ways:

■ The host device can connect a GPIO to the HW_RESET of BoT-cDA110 module and pull HW_RESET low until VDD is stable. HW_RESET is recommended to be released 50ms after VDD is stable.

■ If the HW_RESET connection of the BoT-cDA110 module is not used in the application, should be not connected to the HW_RESET solder pad of the BoT-cDA110 in order to delay the HW_RESET release by internal RC delay circuit. Internal RC delay time may differ depending on the VDD power supply ramp time of the system. The RC delay time should result in an HW_RESET release timing of at least 50ms after VDD stability.

■ The HW_RESET release timing may be controlled by a external voltage detection IC. HW_RESET should be released 50ms after VDD is stable



<RESET Timing>

3.3. UART Interface

This is a standard UART interface for communicating with other serial devices.

BoT-cDA110 UART interface provides a simple mechanism for communicating with other serial devices using the RS-232 protocol.

When BoT-cDA110 is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices. The remaining 2 signals, UART_CTS and UART_RTS, implement optional RS232 hardware flow control where both are active low indicators.

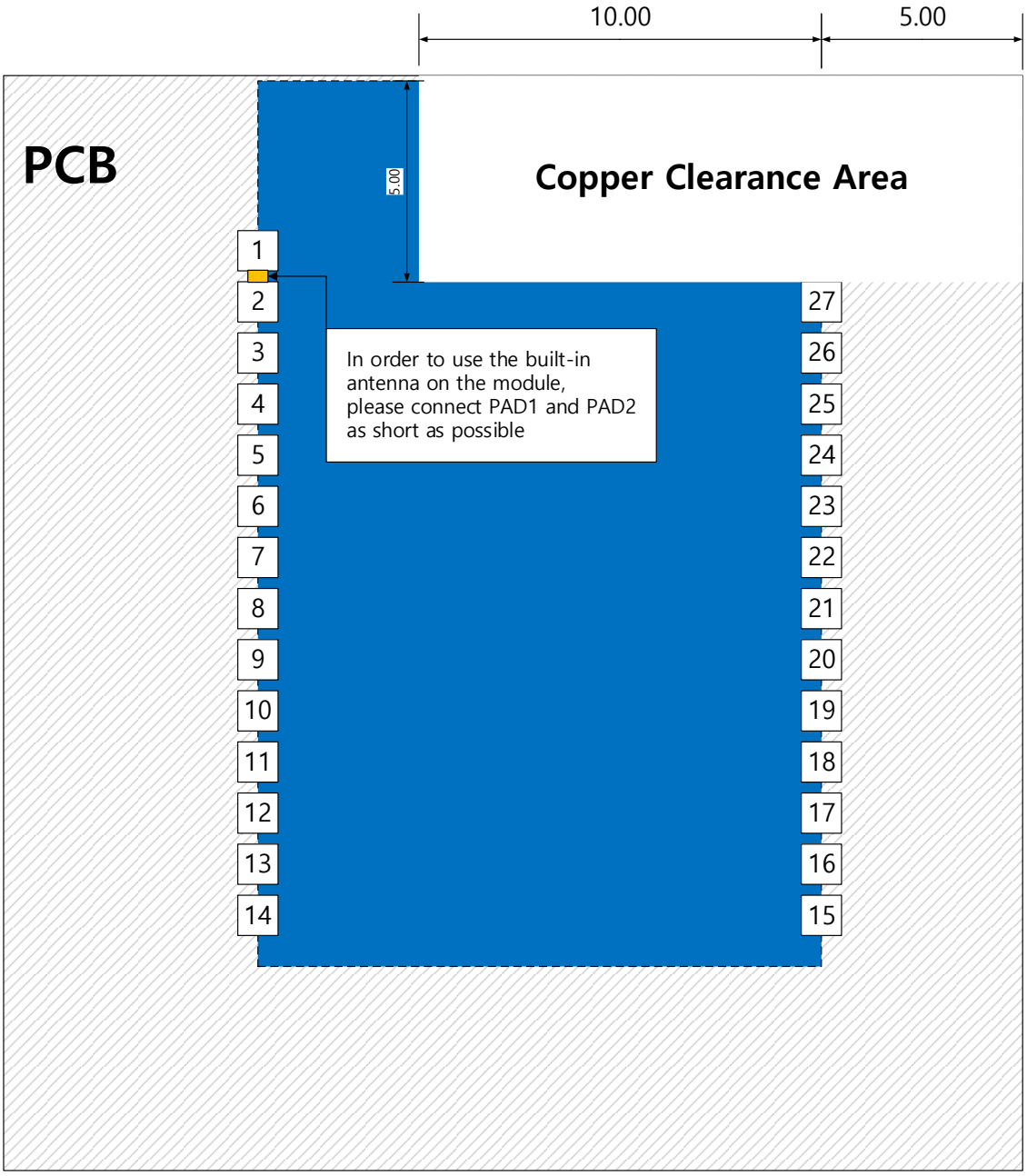
UART configuration parameters, such as baud rate and packet format, are set using BoT-cDA110 firmware.

Configuration Parameters	Supported Value
Data Length	8 bit
Flow Control	Hardware RTS/CTS None
Parity	Even Odd None
Number of stop bit	1 or 2
Baud rate	9600 19200 38400 57600 76800 115200 230400 460800

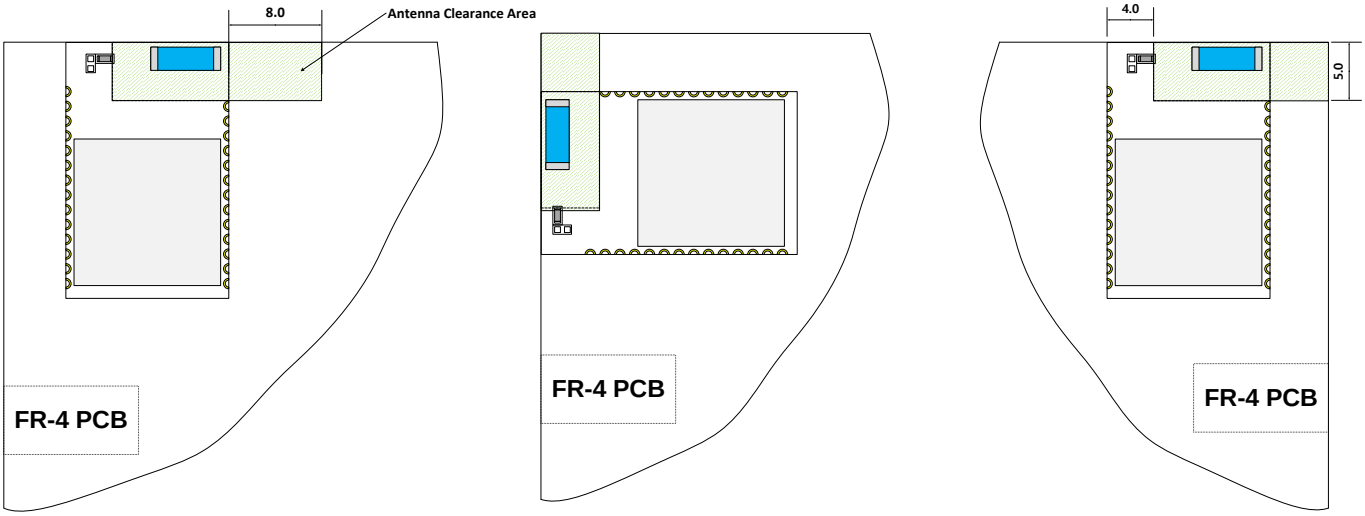
<UART Configuration List>

4. Internal Antenna

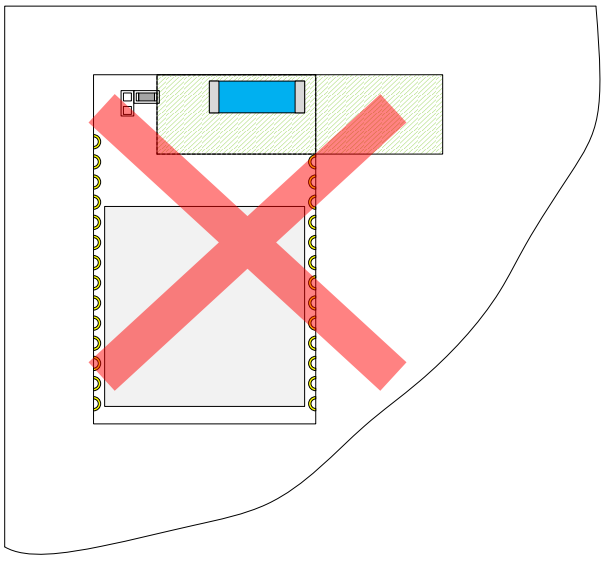
4.1. Antenna Layout Guide



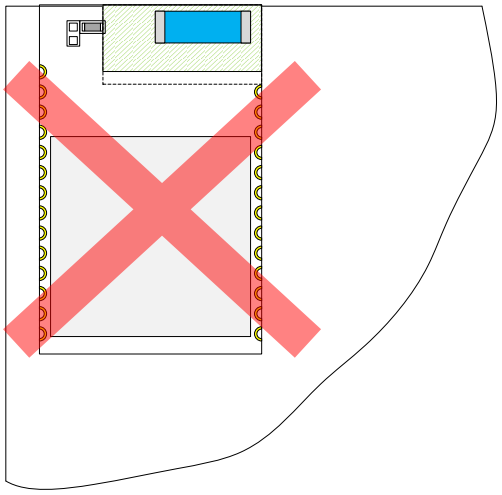
4.2. Recommended Module Mounting



Recommended Module Mounting Example



Antenna 영역을 GND가 둘러싸고 있는 형태



Antenna 영역을 크기를 축소 하거나
Antenna 영역에 GND가 겹치는 형태

Wrong Module mounting Example

5. Reflow Temperature profile

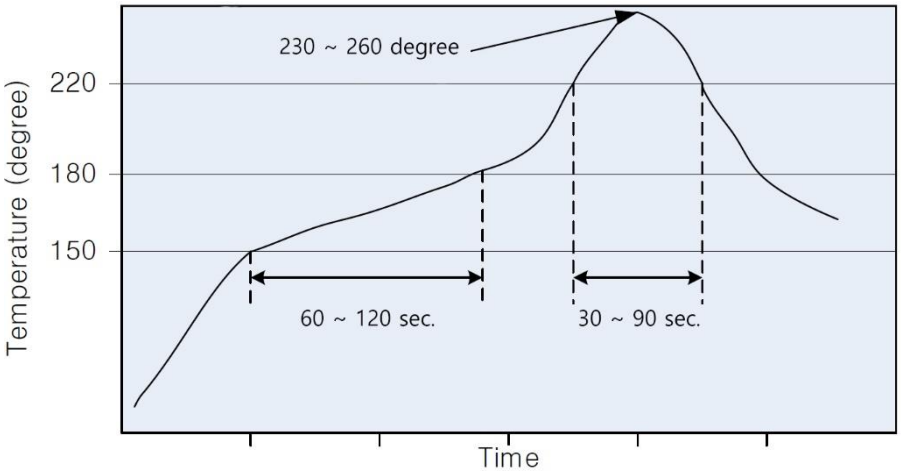
Recommended solder reflow profile are shown in below and follow the lead-free profile I accordance with JEDEC Std. 20C.

Table lists the critical reflow temperatures.

Flux residue remaining from board assembly can contribute to electrochemical migration over time.

This depends on number of factors, including flux type, amount of flux residue remaining after reflow, and stress conditions during product use, such as temperature, humidity, and potential difference between pins.

Care should be taken in selecting production board/module assembly processes and materials, taking into account these factors.

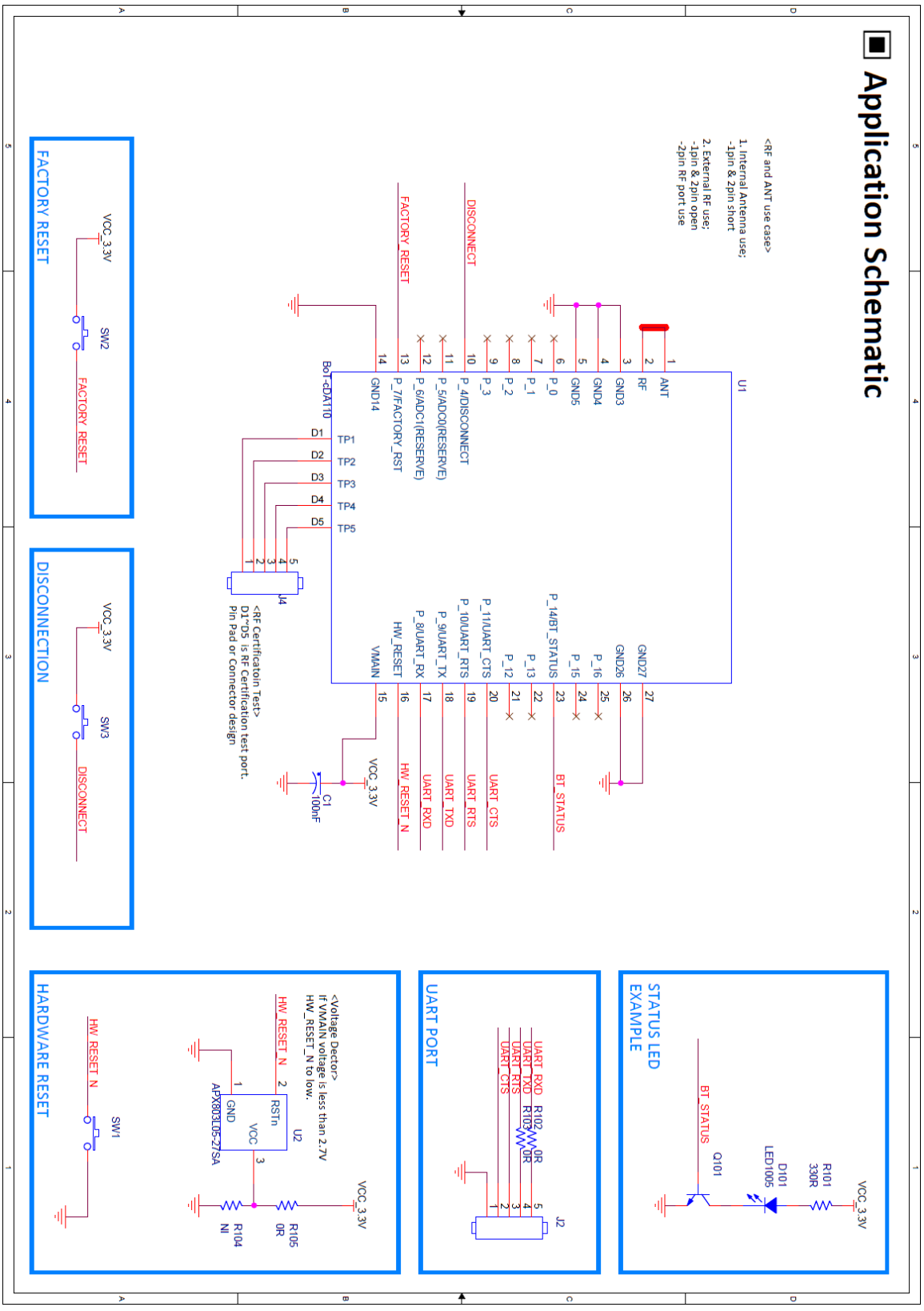


Process Step	Lead-Free Solder
Ramp rate	3°C/sec
Preheat	Max. 150°C to 180°C, 60 to 180 sec
Time above liquidus	+220°C 30 to 90 sec
Peak temperature	+255°C ±5°C
Time within 5°C of peak temperature	10 to 20 sec
Ramp-down rate	6°C/sec max

WARNING: For BoT-cDA110.

If you have reflow process multiple times in your product, you must be proceed this module in the final reflow process. If not the Shield can will drop out if shield-can adopted.

6. Application Schematic



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